

Turis 14" 15" 2SP Schematic

Apollo Lake

2016-09-07
REV : A00

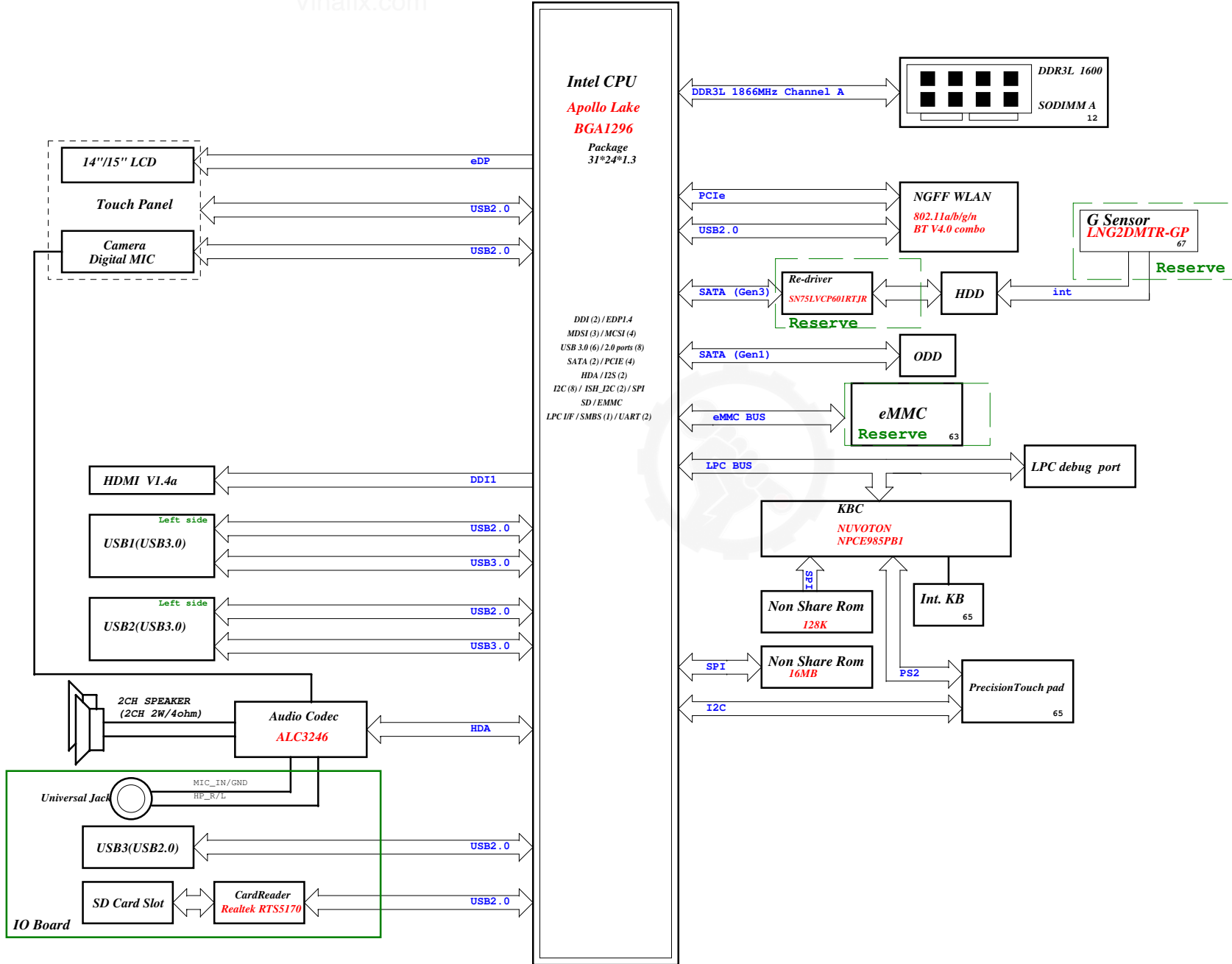
DY : None Installed
UMA: UMA only installed

<Core Design>

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Title			
Cover Page			
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TURIS 14" 15" 2SP Apollo Lake Block Diagram

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CHARGER		
BQ24727R6RR	44	
INPUTS	OUTPUTS	
19V_DCBATOUT	BT-	
SYSTEM DC/DC		
TPS51225RUKR	45	
INPUTS	OUTPUTS	
19V_DCBATOUT	3D3V_AUX_S5	
	3D3V_S5	
	5V_S5	
CPU DC/DC PMIC		
RT9610BZQW	50	
INPUTS	OUTPUTS	
5V_S5	1D05V_S0	
	1D8V_S5	
	1D24V_S5	
035V_CPU_VDDQ_S3	00675V_CPU_VDDQ_S3	
CPU DC/DC PMIC		
RT9610BZQW	51	
INPUTS	OUTPUTS	
5V_S5	1V_CPU_VNN	
	1V_CPU_VCGI	
	1D35V_CPU_VDDQ_S3	
SYSTEM LDO		
APL3523AQBI	40	
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
SYSTEM LDO		
TPS22965DSGR	40	
INPUTS	OUTPUTS	
1D8V_S5	1D8V_S0	
PCB LAYER		
L1:Top		
L2:VCC		
L3:Signal		
L4:Signal		
L5:GND		
L6:Bottom		


SSID = CPU

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SSID = CPU

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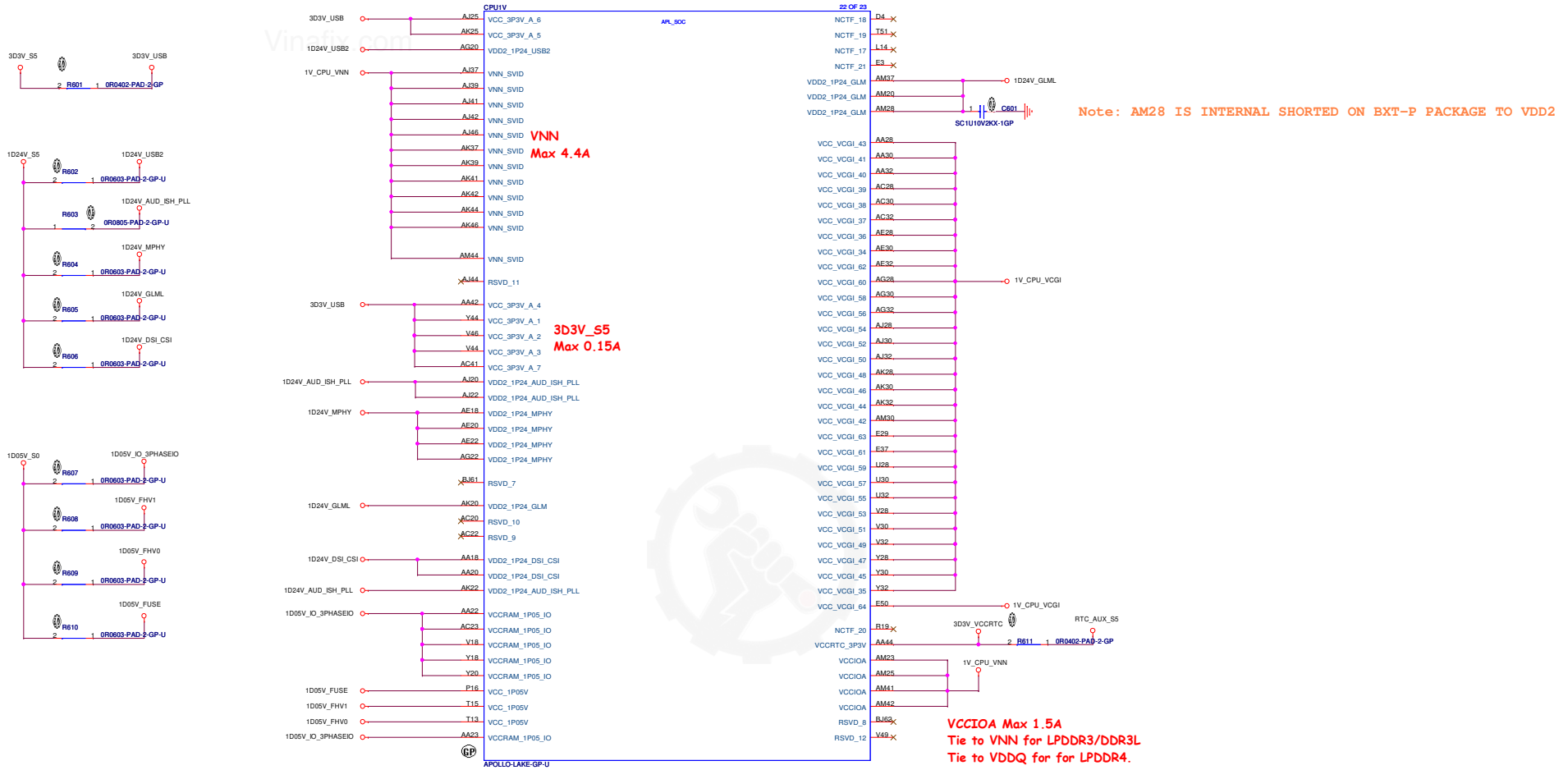


Table 11. SoC and Platform Voltage Rails

Package Pin Name	Voltage @ Pin (V)	Type	Internal Logic	ICCMAX (A)
VCC_1P24V_1P35V_A	1.24 - 1.35	Fixed	L2, PLLs, IO: USB2, USB3, SATA, PCIe, SSC, Debug port, SDIO SRAMs & PLLs	1.3
VCC_3P3V_A	3.30	Fixed	1PP Fuse, USB2 IO	0.15
VCCRTC_3P3V	2 - 3.30	Fixed	RTC	

Package Pin Name	Voltage @ Pin (V)	Type	Internal Logic	ICCMAX (A)
VCC_VCGI	0, 0.45 - 1.24	IMVP8 SVID or I2C	CPU Cores, GFX cores, I-Unit	21
VNN	0, 0.45 - 1.24	IMVP8 SVID or I2C	SA, D-Unit, I/O controllers, DDR3L/ LPDDR3 PHY Logic DLL	4.4 (LPDDR3 & DDR3L)
VCC_1P05V	1.05	Fixed	S0 SRAM, Graphics, Fuse Sensing, IO logic (HDM1, eDP, USB2, SSC, PCIe, MIPI-CS13)	2.7
VCC_1P8V_A	1.80	Fixed	IO: USB2, JTAG/ITP, CFIO, UART, PWM, SPI, I2C, SDIO, eMMC	0.4
VDDQ	1.24 (LPDDR3) 1.35 (DDR3L)	Fixed	LPDDR3 IO DDR3L IO	2.8 (excluding DRAM)
VCC_1P24V_A	1.24	Fixed	IO: MIPI-DSI, MIPI-CSI	1.3

SSID = CPU

[50] VSS_VCCGI <<<
[50] FB_VCCGI <<<
[50] FB_VNN <<<

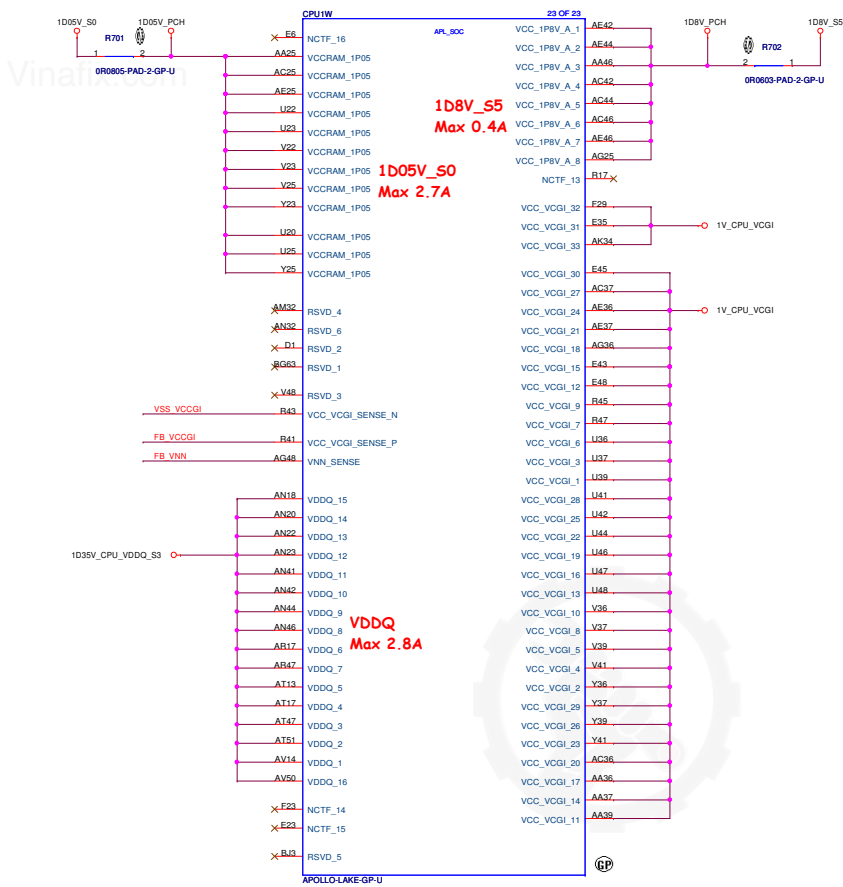
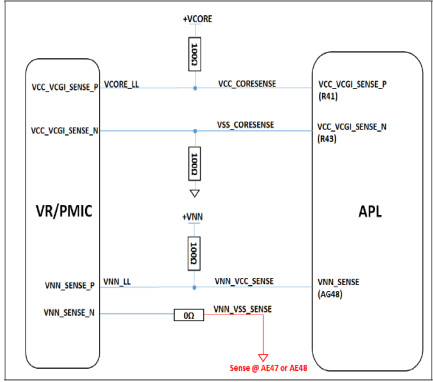


Figure 3-4. VCGI, VSS, VNN Sense Guideline



HDMI

```
[57] HDMI_DATA_CUPL_P2 <<<
[57] HDMI_DATA_CUPL_P2 <<<
[57] HDMI_DATA_CUPL_P1 <<<
[57] HDMI_DATA_CUPL_P1 <<<
[57] HDMI_DATA_CUPL_P0 <<<
[57] HDMI_DATA_CUPL_P0 <<<
[57] HDMI_DATA_CUPL_P3 <<<
[57] HDMI_DATA_CUPL_P3 <<<
[57] HDMI_DATA_CUPL_P3 <<<
```

[57] HDMI_CLK_CPU <<>>

[57] HDMI_DATA_CPU <<>>

[57] HDMI_DET_CPU >>>

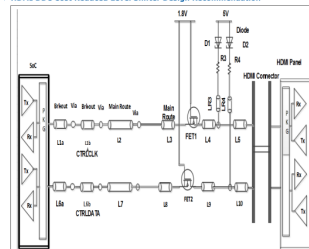
EDP

```

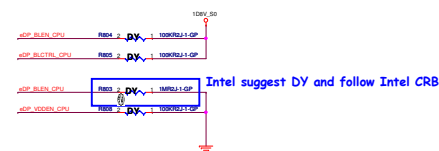
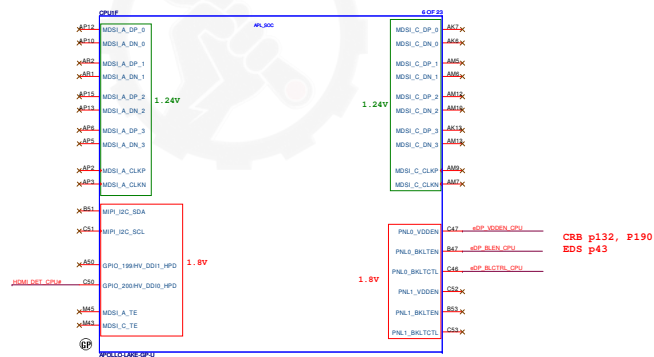
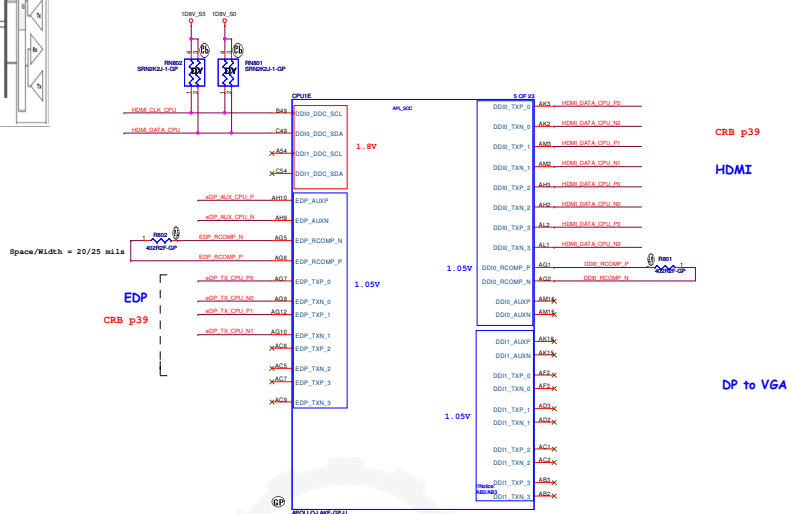
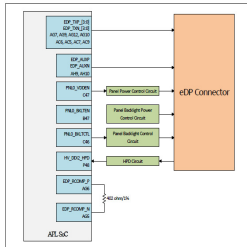
[50] eDP_AUX_CPU_P <<<
[50] eDP_AUX_CPU_N <<<
[50] eDP_TX_CPU_P0 <<<
[50] eDP_TX_CPU_N0 <<<
[50] eDP_TX_CPU_P1 <<<
[50] eDP_TX_CPU_N1 <<<
[24,55] eDP_VDDEN_CPU <<<
[55] eDP_BTCTRL_CPU <<<
[24] eDP_BLEN_CPU <<<

```

HDMI DDC Cost Reduced Level Shifter Design Recommendation

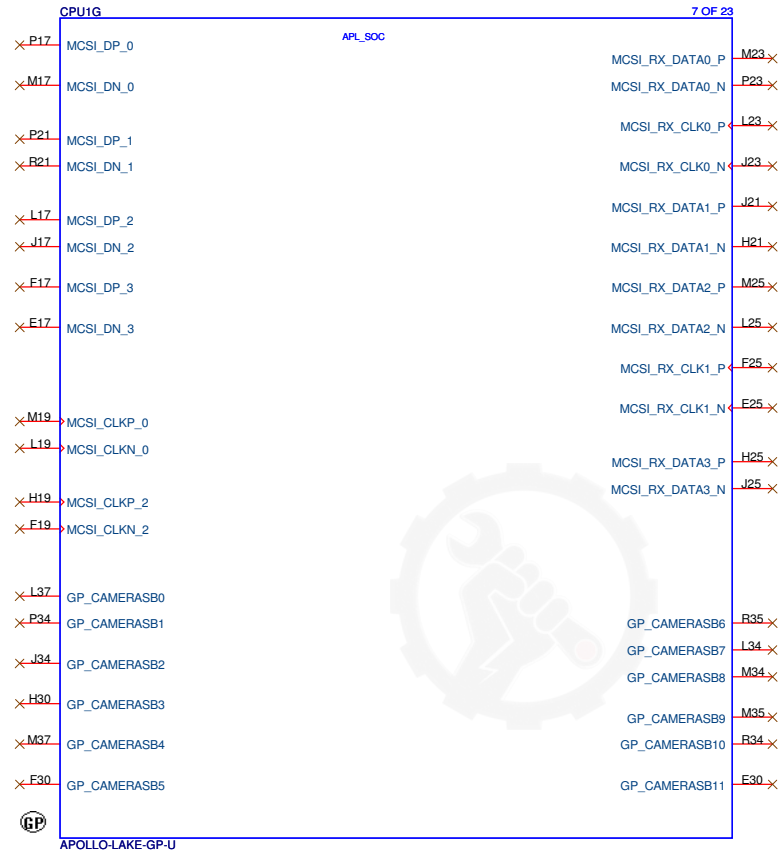


eDP® Channel



SSID = CPU

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Title CPU (VSS)			
Size A3	Document Number Turis APL UMA	Rev X02	
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SSID = CPU

VCCGI

IccMax = 21 A

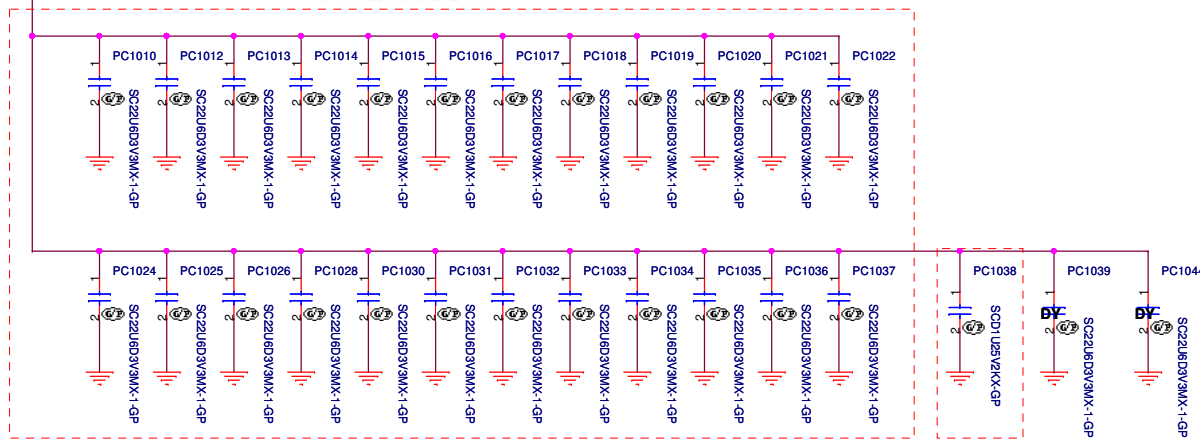
CRB: 1U 0402 x 12, 22U 0603 x 8, 47U 0805 x 10 CRB p56

0.1U 0402 x 1

22U 0603 x 24, DY x 4

follow power team

1V_CPU_VCGI



1D05V_IO_3PHASEIO

22U 0603 x 1

1D05V_PCH

22U 0603 x 2

System Rail Name	Power Rails [GND]	Max L from Ball to nearest BSC			Max L from Ball to nearest ESC			Max L from Ball to nearest MLCC			Max L / R from Ball to VR Bulk		
		Back Side Cap	BSC (nH)	Total (nH)	Top Side Edge Cap	ESC (nH)	Total (nH)	Top Side MLCC	MLCC (nH)	Total (nH)	Top Side Bulk	Bulk (nH)	(mΩ)
VCCRTC_3P3V	AA44 [Y46]							1 X 0603 22uF	C3P1	5.88		6.83	20.52

VNN

1V_CPU_VNN

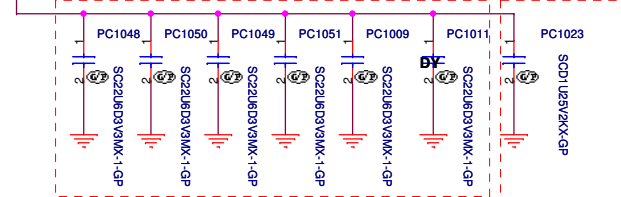
CRB: 1U 0402 x 3, 22U 0603 x 4

22U 0603 x 4, DY x2

0.1U 0402 x 1

follow power team

+VCCSA (ICCMAX.=6A)



1D24V_MPHY

PC1046

1D8V_PCH

PC1101

1D24V_DSI_CSI

PC1102

1D24V_GLM

PC1043

1D24V_AUD_ISH_PLL

PC1042

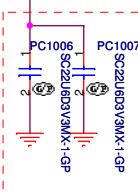
3D3V_USB

PC1103

(VNN) for 1V_VCCIOA

1V_CPU_VNN

22U 0603 x 2

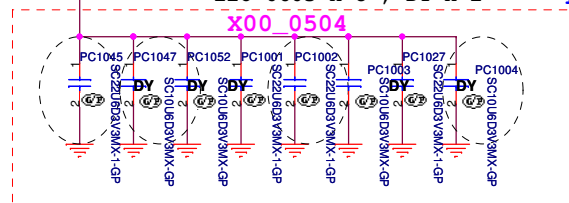


1D35V_CPU_VDDQ_S3

0.1U 0402 x 1

22U 0603 x 8, DY x 2

follow CRB



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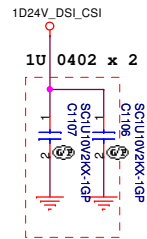
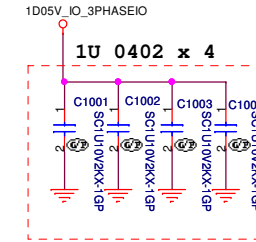
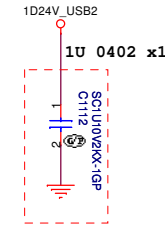
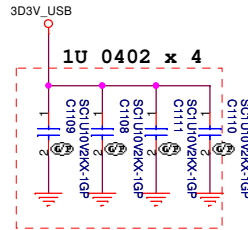
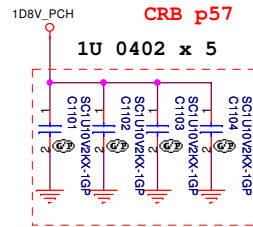


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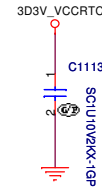
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CPU (Power CAP1)				
Size A3	Document Number			Rev
Turis APL UMA			X02	
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SSID = CPU

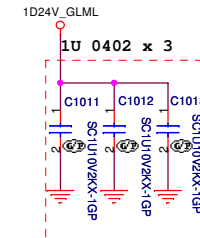
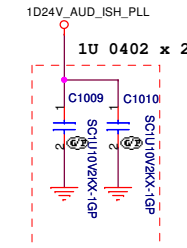
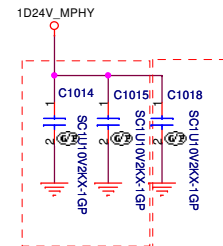
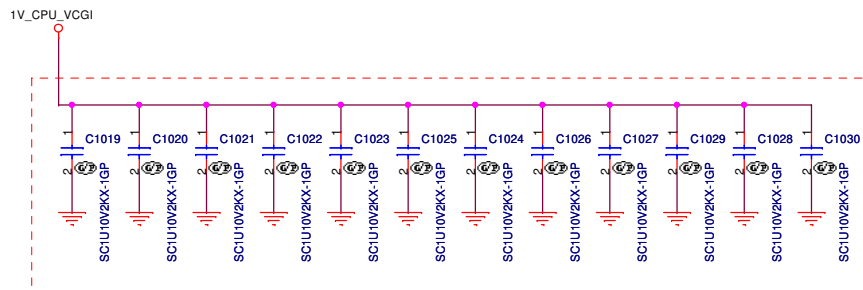
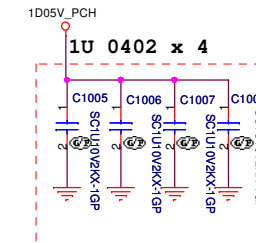
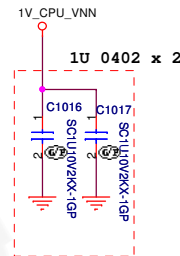
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change from INTEL 559091 MOW Page 4



(VNN) for 1V_VCCIOA



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Title			
CPU (Power CAP2)			
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DDR_DATA

[2] M_A_DQ25_DIN[7:0] <<>>

[2] M_A_DQ25_DIP[7:0] <<>>

[2] M_A_DQ[53:0] <<>>

[2] M_A_A[15:0] <<>>

DDR CMD/ADD

(5) M_A_RAS#

(5) M_A_WE#

(5) M_A_CAS#

(5) M_A_B52

(5) M_A_B50

(5) M_A_B51

DDR CTRL

[5] M_A_CS#0                                                                                                                                     

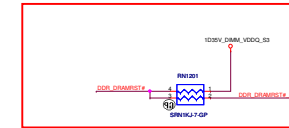
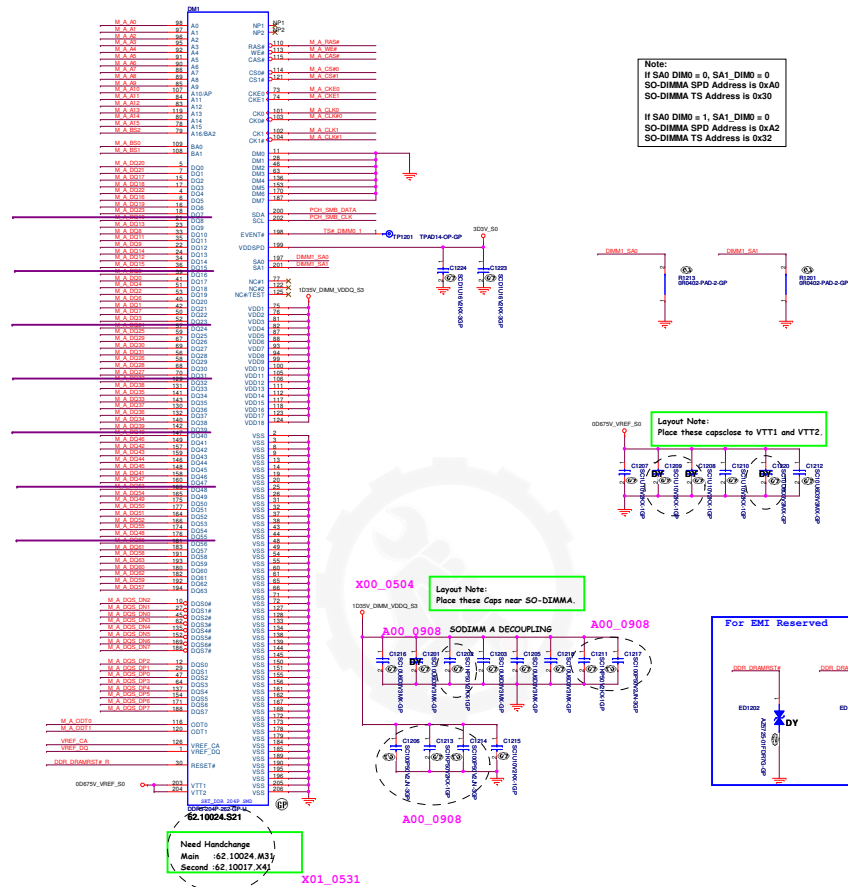
DDR CLOCK

[5] M_A_CLK0
[2] M_A_CLK0

[5] M_A_CLK1
[2] M_A_CLK1

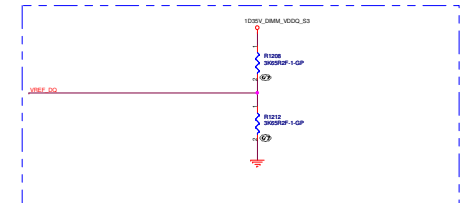
DDR OTHERS

[5] DDR_DRAMFST# >>>
[17,65,70] PCH_SMB_DATA <<<
[17,65,70] PCH_SMB_CLK <<<

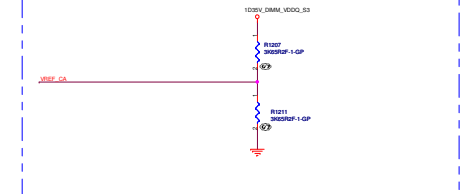


For Intel Recommend Close to DIMM

The design of Vref refer to PDG rev.1.0.



For Intel Recommend Close to DIMM




SSID = MEMORY

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SSID = CPU


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SSID = STRAP

GPIO	GPIO_36	GPIO_39	GPIO_43	GPIO_44	GPIO_47	GPIO_78
Schematic						
High	VCCIO used for B-step	enable CSE ROM bypass	RSVD	default (allow SPI as a boot source) Weak internal pull-up	force DNX FW Load	SMBus 1.8V mode select
Low	default (A-step) Weak internal pull-down	default (disable bypass) Weak internal pull-down	Weak internal pull-up	disable	default (don't force DNX FW Load) Weak internal pull-down	SMBus 3.3V mode select Weak internal pull-up

GPIO	GPIO_88	GPIO_92	GPIO_111	GPIO_110	GPIO_118	GPIO_120
Schematic						
High	FW 1.8V mode select	SMBS No-reboot enable	Do not boot from SPI Weak internal pull-up	LPC 1.8V mode select	Flash Descriptor Override	Two SWAP override enable
Low	FWB 3.3V mode select Weak internal pull-up	default (SMBus No Re-Boot Disable) Weak internal pull-down	boot from SPI	LPC 3.3V mode select Weak internal pull-up	No Override (Normal Operation) Weak internal pull-down	default (Disable top swap override) Weak internal pull-down

GPIO	GPIO_123					
Schematic						
High	RSVD (Internal 10K PU)					
Low	RSVD					

Table 2-36. Hardware Straps

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_36	VCC_1P04V_1P35V_A voltage selection	20K PD	1 = 1.35V 0 = 1.24V (default) Note: This strap will only be used for B-step. For A-step this ratio should only be set at 1.24V
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) Note: North Lake supports TXX3.0 (this is also called CSE) Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXX3.0) before the first patch point this strap enables the platform tell CSE (TXX3.0) to bypass the ROM causing the issue and go to the patch source instead.
GPIO_40	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_43	Allow eMMC as a boot source	20K PU	1=enable (default) 0=disable
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) Note: DNX: Download and Execute Note: This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXX3.0) to execute a "Download and Execute" (DNX) flow where it would load firmware from a USB stick and re-flash a USB CSE (TXX3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.

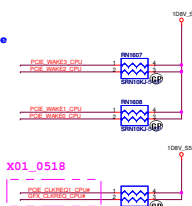
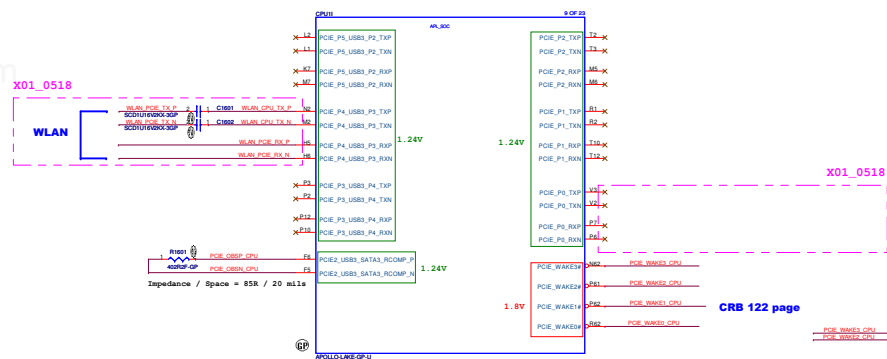
GPIO_48	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) Note: Platforms should strap this LOW. Functionality is handled by the PMC.

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_104	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_111	Boot BIOS Strap (BBS)	20K PU	1 = Do not boot from SPI (default) 0 = Boot from SPI
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override Note: This strap enables the platform to override security features in the SPI.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_117	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

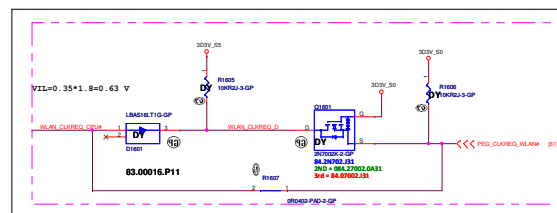
Note: All the straps are sampled at Rising Edge of RSM_RST_N

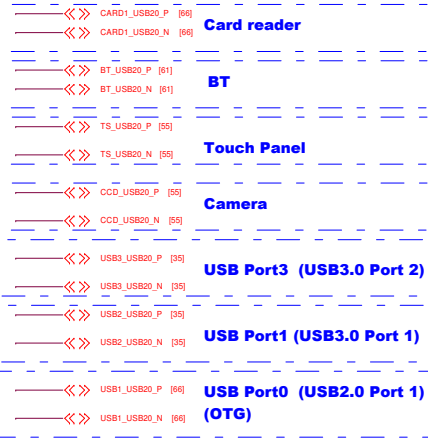
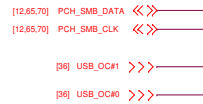
6	SATA 3.0 P0	
7	SATA 3.0 P1	USB 3.0 P1
8	PCIe P1	
9	PCIe P2	
10	PCIe P0	
11	USB 3.0 P4	PCIe P3
12	USB 3.0 P3	PCIe P4
13	USB 3.0 P2	PCIe P5
14	USB 3.0 P1	
15	USB 3.0 P0	

High Speed I/O (HSIO) Lane Multiplexing in APL SoC



WLAN and LAN side are OD pin,
so no need LS



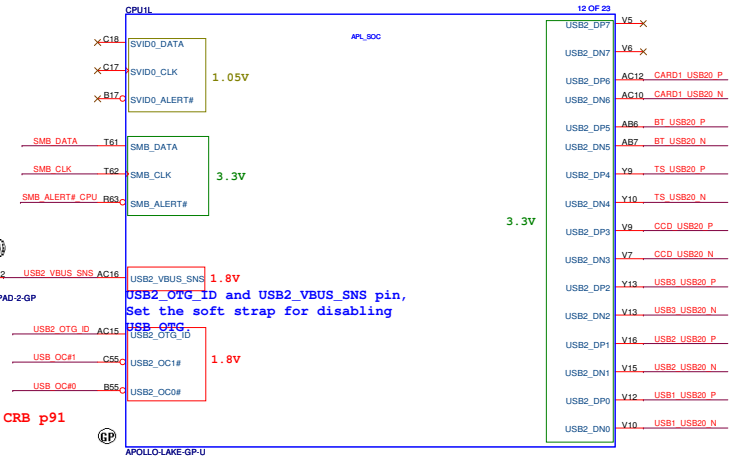
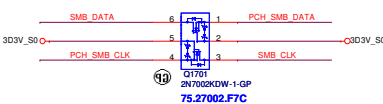
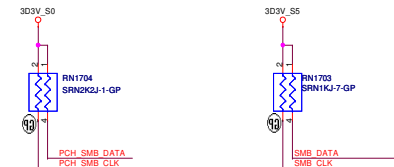
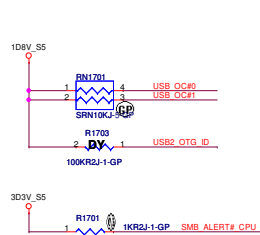


CPU and VR side both PU 170R, and damping 20R close VR
Only VR side PU 85R, and damping 95R close VR
Only CPU side PU 68R, and damping 220R close CPU

PDG1.2

10.10 USB 2.0 Disabling and Termination Guidelines

- If a USB port(s) is not implemented on the platform:
- USB2_DP [7:0] and the USB2_DN [7:0] signals can be left unconnected
 - USB2_OC[x].N pins needs to be terminated with internal pull ups, which are enabled by default
 - When the platform does not use the USB2_OTG_ID and USB2_VBUS_SNS pins, USB2_OTG_ID pin should be unconnected on the platform (terminated with internal pull ups) and USB2_VBUS_SNS should be connected to ground
 - USB2_RCOMP needs to be connected to 113 ohms 1% resistor pull down resistor



- Card reader
- BT
- Touch Panel
- Camera
- USB Port2 (USB3.0 Port 3)
- USB Port1 (USB3.0 Port 2)
- USB Port0 (USB2.0 Port 1) (OTG)

Table 61. Over current Pin Default Usage

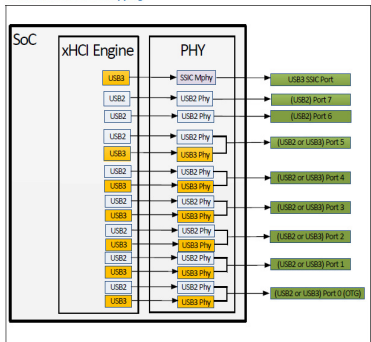
Pin	Default Port Mapping
OC0#	Port 0
OC1#	Port 1-7

Table 62. Over current Pin Example Configuration

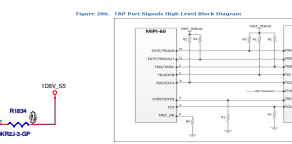
Location	Number of USB Ports	USB Ports Number	OC Pins Used
External Topology	1	0	OC0#
External Topology	4	1,2,3,4	OC1#

NOTE: All USB ports routed out of the package must have over current protection. It is the system BIOS responsibility to ensure all used ports have OC protection.

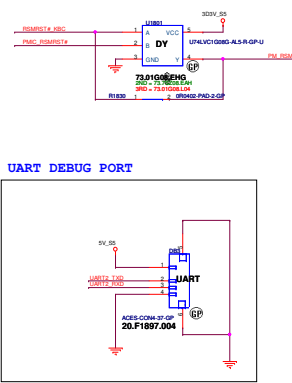
Figure 3-3. USB2 and USB3 Port Mapping



Notes: There are 8x USB Ports supported on Apollo Lake. USB Ports [5:0] can be used as USB2 and USB3 and are mutually exclusive. USB Port 6 and Port 7 can only be used as USB2.

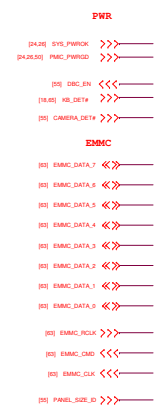
[illegible]

Component Symbol	Component Value
R1	51 Ohm +/- 5%
R2	100 Ohm +/- 5%
R3	100 Ohm +/- 5%
R4	10K Ohm +/- 5%
VREF_DEBUG	1.8V_SUS (VDD1)



SSID = PCH

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CRB p52

X01_0616

X01_0616

X01_0616

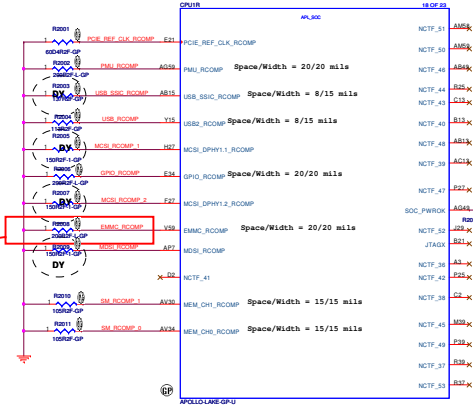
X01_0616

EMMC_RCOMP Signal Routing General Layout Requirement

Trace length : 500-1000

Trace width : 20 mils

Isolation to other signal: 8mils

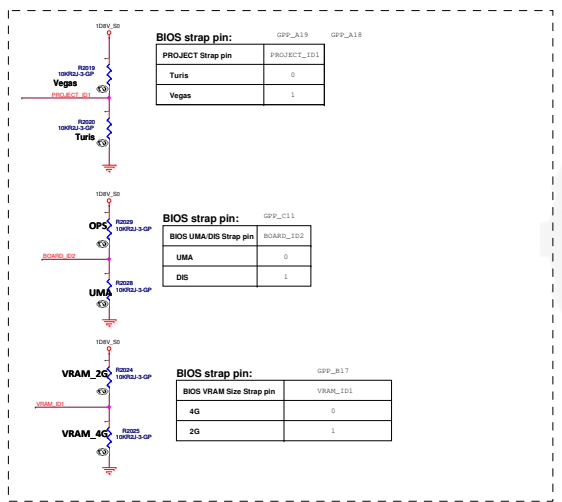


all S0 power rail ok (PWR_PWR0K)
"delay 1D05V_S0 between 5-100ms"
(input_pin)

CRB p52

EDS p35

If the SOC_PWR0K signal is connected to the EC then in the G3 state the EC is turned off and there is no termination for the SOC_PWR0K signal. Floating SOC_PWR0K signal in G3 State can cause high leakage in the RTC 3.3V rail. To address this, please make sure there is a weak pull down (~100 kohm) path to GND for SOC_PWR0K in G3 State to ensure low leakage on RTC. From M0M44



BIOS strap pin: GPP_A19 GPP_A18

PROJECT Strap pin	PROJECT_ID1
Turis	0
Vegas	1

BIOS strap pin: GPP_C11

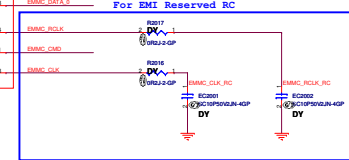
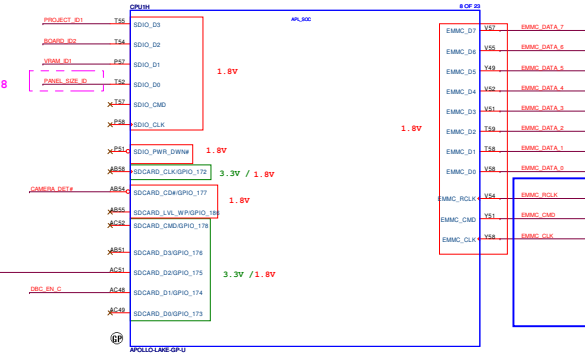
BIOS UMADS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin: GPP_B17

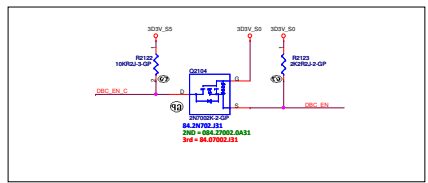
BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

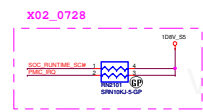
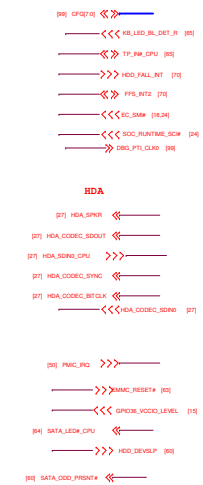
X02_0718

CRB P64



Level Shift

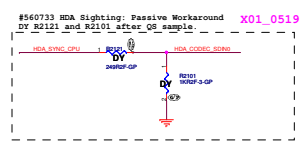
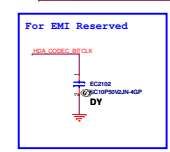




ISH INT: Active low, OD

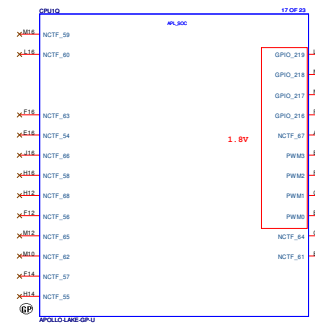
EDS p42

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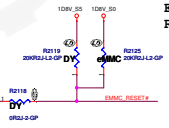


1206618869: HD Audio SDI I/O Pin Issue

- Problem: The SDI signal Pin on Apollo Lake SoC has been configured as Input only.
- Implication: The HDA SDI signal Pin on SoC is incorrectly configured as Input-Only, instead of I/O. As a result of this issue, this Pin can not be driven by the SoC during initialization phase, thus making external HD Audio Codec un-detectable by the Audio driver. However, HDMI and QS audio are not affected.
- Workaround: Intel recommends customers to implement the temporary hardware workarounds listed in the next slide on their platforms. Customers can remove (un-stuffed) the workaround when this issue is fixed in [QS sample](#).
- Status: Plan Fix.

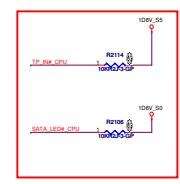


EDS1.0 Page 52 QS Sample can Support R2119, R2118 stuff and DY Q6301, R2125

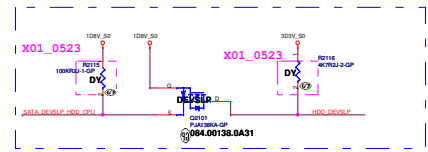


CRB p49

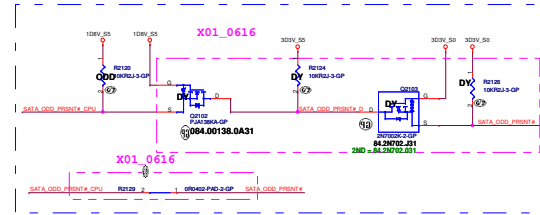
Serial ATA Port [0] General Purpose Inputs (SATA_GP0): When configured as SATA_GP0, this is an input pin that issued as an interlock switch status indicator for SATA Port 0. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.



DEVSUP



ODD PRSNT



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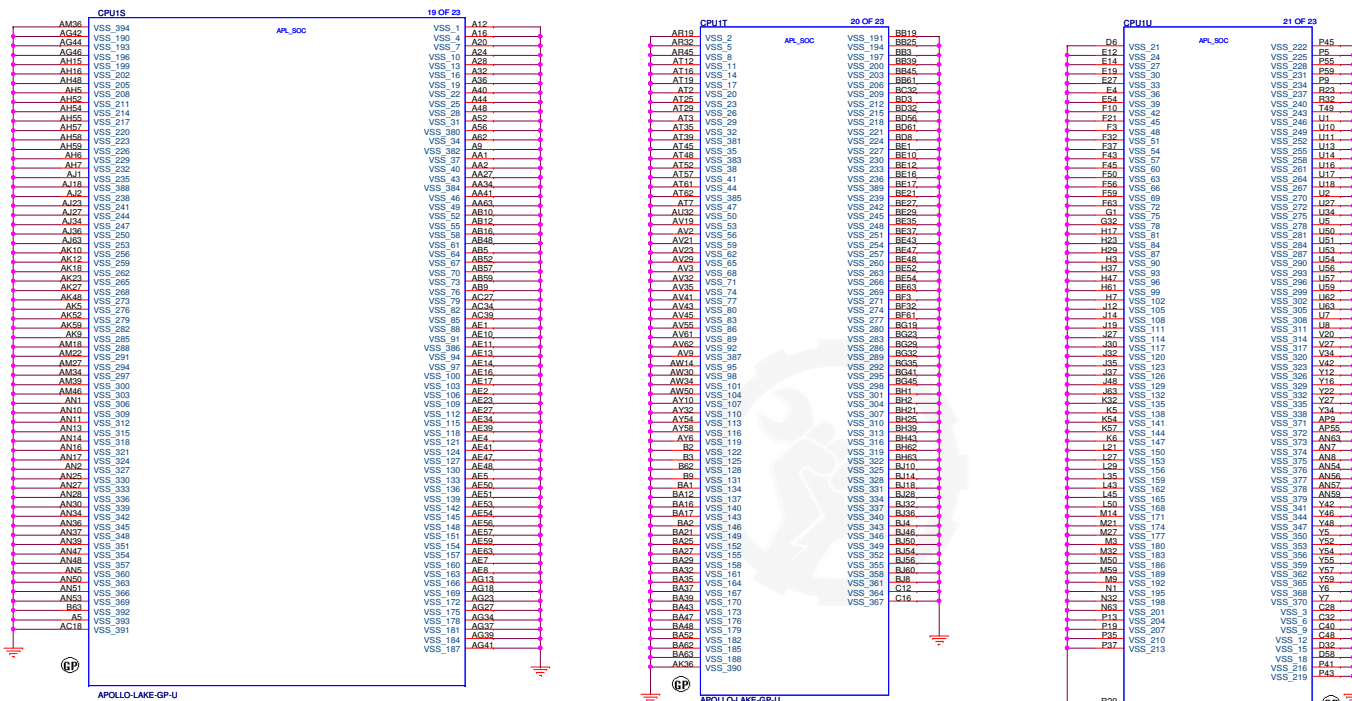
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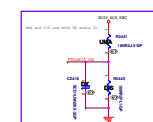
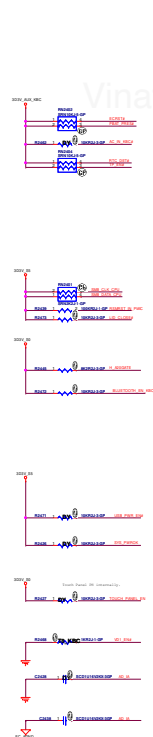
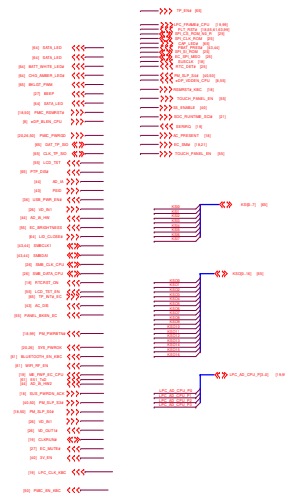
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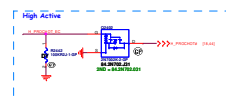
SSID = CPU

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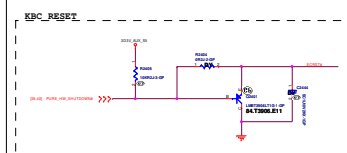
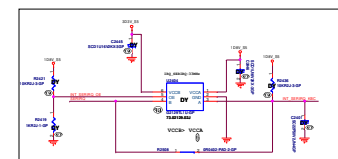
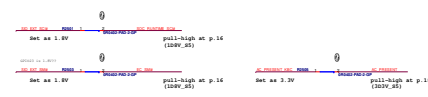
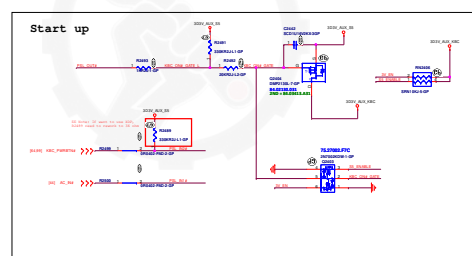
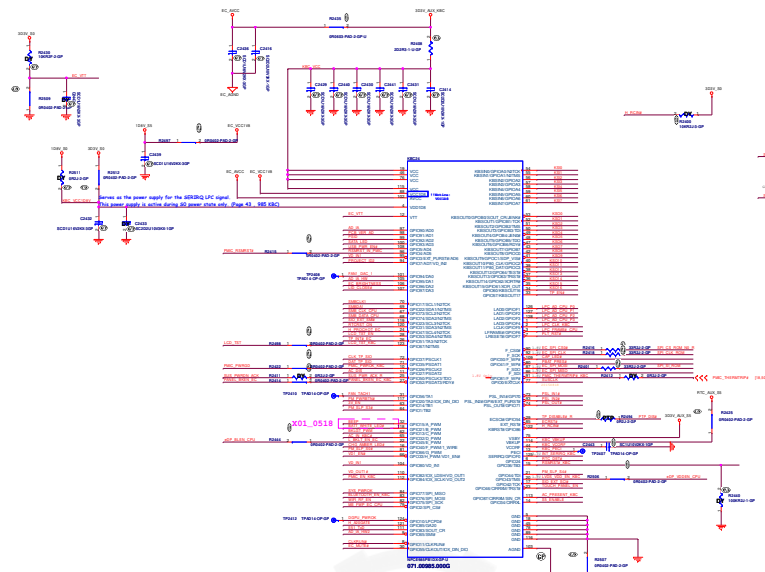




	PROJECT_ID2
UMA	H
DIS	L



MSL, 100% (a)	Pre-Live Scenario	Full-Live Scenario	Current College	Live College	Live College	MSL Premium Setting
GA	100.0%	92.0%	2,050.0	2,050	2,045	>= 2.05 V
SD	100.0%	30.0%	2,270.0	2,270	2,240	>= 2.07 V
TX	100.0%	10.0%	2,440.0	2,440	2,400	>= 2.03 V
AL	100.0%	47.0%	2,240.0	2,250	2,225	>= 2.02 V
Reserved for project use	100.0%	84.0%	2,011.0	2,019	1,984	>= 2.01 V
Reserved for project use	100.0%	70.0%	1,937.0	1,937	1,905	>= 1.75 V
Reserved for project use	100.0%	100.0%	1,052.0	1,060	1,035	>= 1.04 V
Reserved for project use	100.0%	144.0%	1,308.0	1,310	1,301	>= 1.01 V
Reserved for project use	100.0%	174.0%	1,234.0	1,237	1,241	>= 1.00 V
Reserved for project use	100.0%	104.0%	1,044.0	1,044	1,039	>= 1.00 V



SSID = Flash.ROM

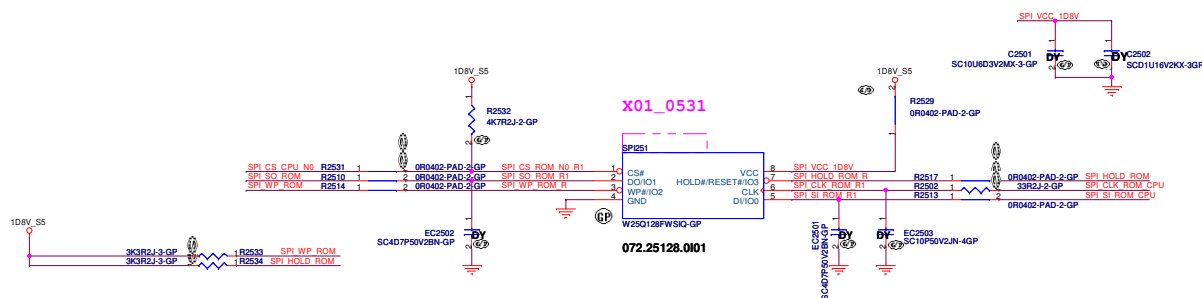
```
[19] SPI_CS_CPU_N0 >>>_____
[19] SPI_SO_ROM <<<_____
[19] SPI_WP_ROM <<>>_____
[19] SPI_HOLD_ROM <<>>_____
[19] SPI_CLK_ROM_CPU >>>_____
[19] SPI_SI_ROM_CPU >>>_____
```

```
[24] SPI_CLK_ROM >>> _____
[24] SPI_SI_ROM >>> _____
[24] EC_SPI_MISO <<>> _____
[24] SPI_CS_ROM_N0_R >>> _____
```

A00_0824

Remove SKT251

SPI Flash ROM(16M) P/N: 072.25128.0I01
2nd P/N: 072.25128.0S01



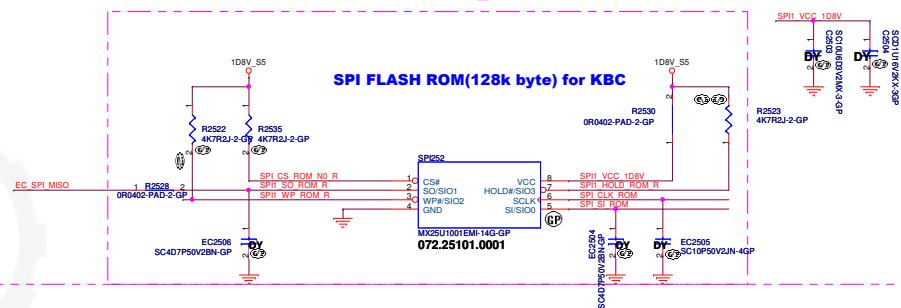
x01 0518

X01_0602

Remove Share Rom

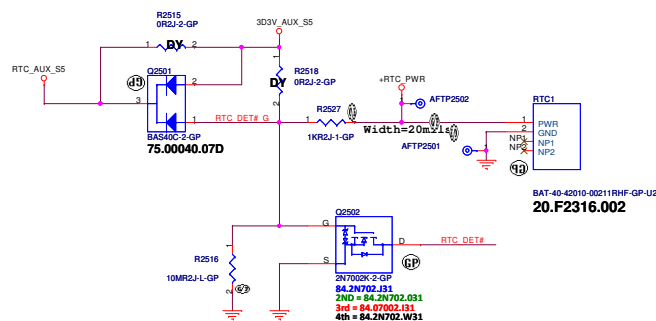
X01_0602

SPI FLASH ROM(128k byte) for KBC



SSID = RTC

————>>> RTC_DET# [24]



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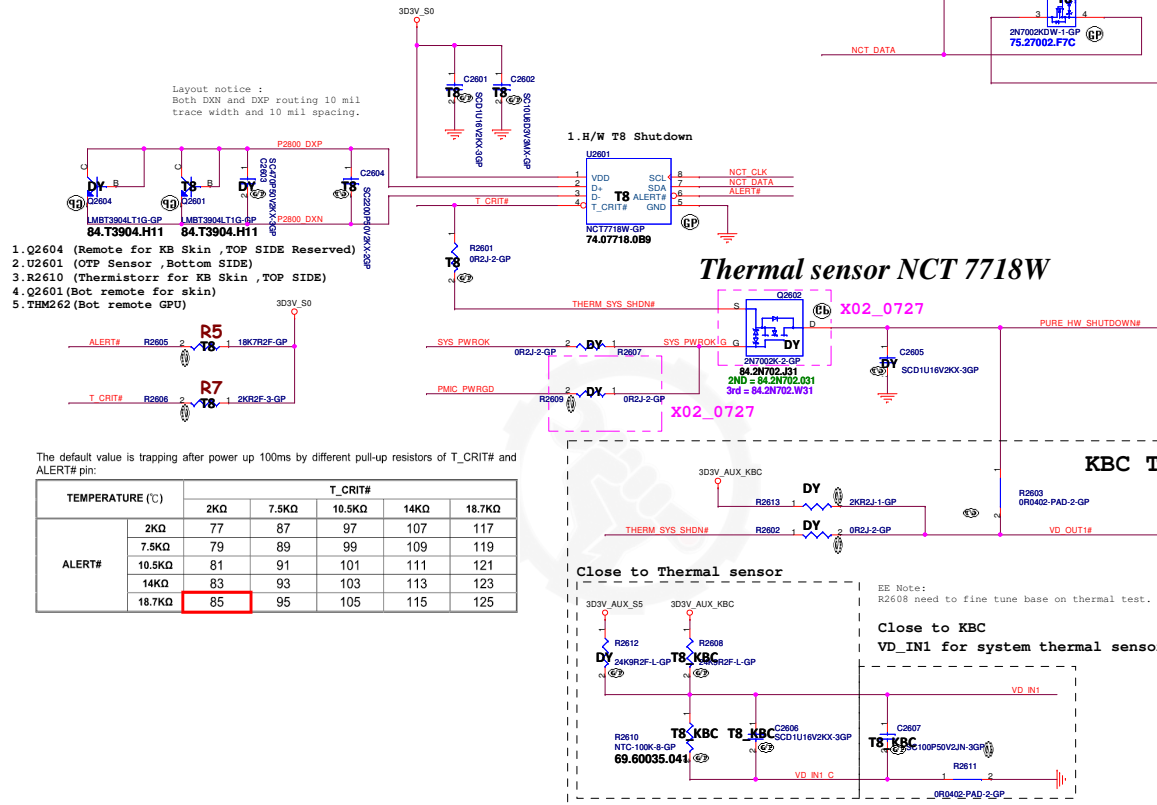
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Flash/RTC			
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EE Note:
 1. T8: PURE_HW_SHUTDOWN# through Q2603.
 2. THM_SENSOR: Thermal sensor NCT7718W solution.

Thermal sensor NCT 7718W

[20,24] SYS_PWROK >>>
 [20,24,50] PMIC_PWRGD >>>
 [24,40] PURE_HW_SHUTDOWN# <<<
 [24] SMB_CLK_CPU <<<
 [24] SMB_DATA_CPU <<<
KBC T8
 [24] VD_OUT1# >>>
 [24] VD_IN1 <<<

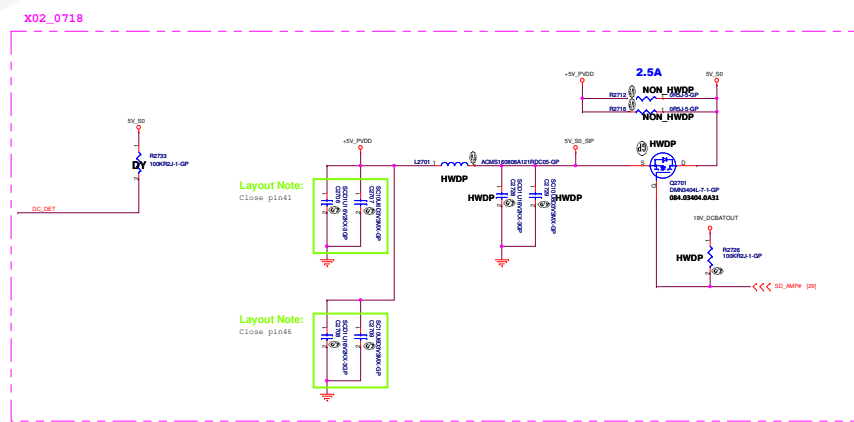


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[illegible]

Power requirement:-
DVDD must >= DVDD IO.

+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support



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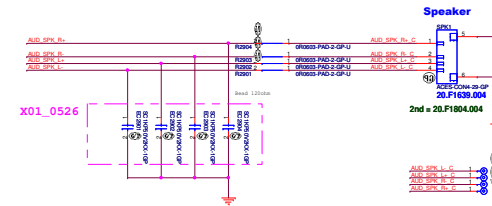
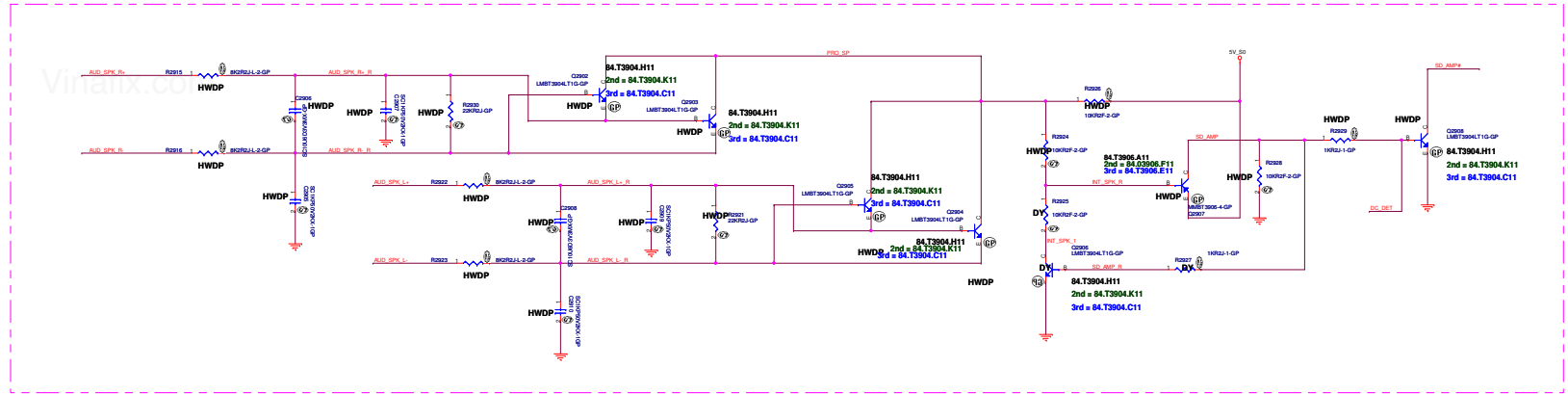
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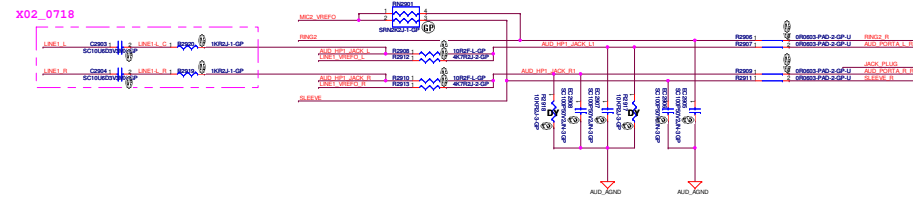
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AUD SPK R+ R2915



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

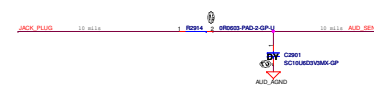
Combo Jack



```

-----
Delay circuit
(JACK_PLUG_DET: on IO Board)

```



Main Func = LAN

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LAN RTL8106

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SSID = LAN CONN

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RJ45+Transformer

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SSID = Card Reader

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Card Reader IC+Reader Conn

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SSID = USB

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Title
(Reserved)USB 2.0 Port

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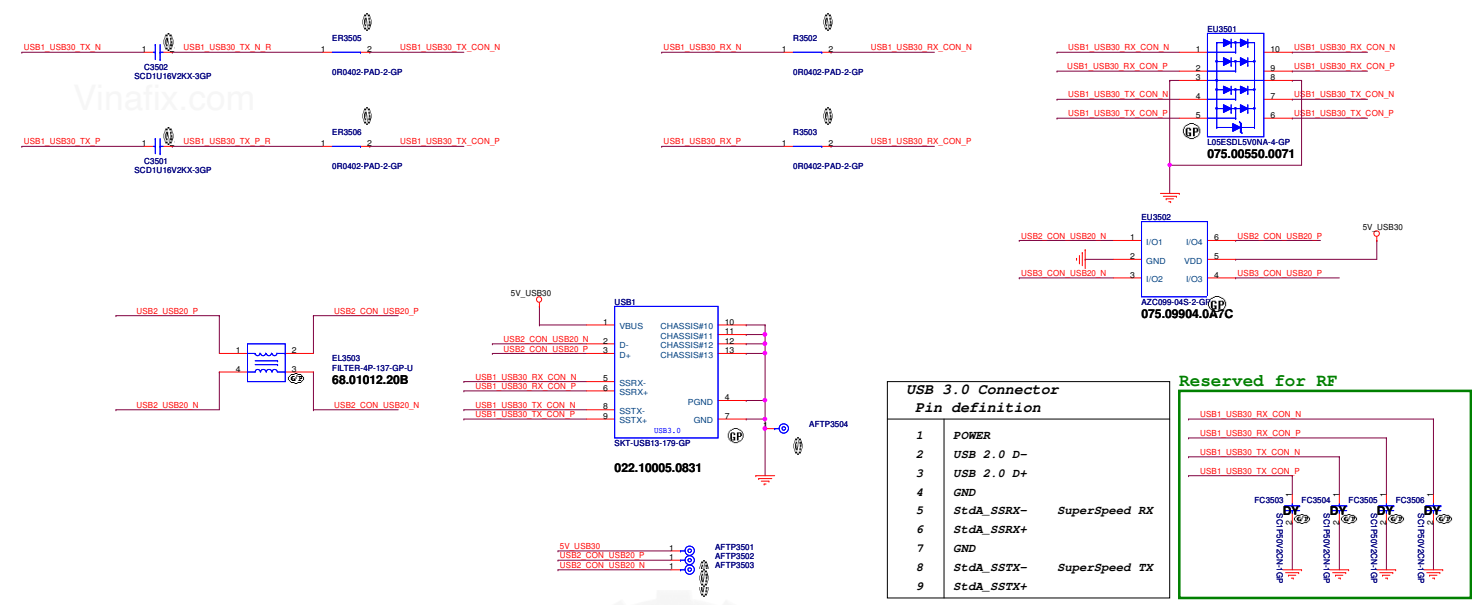
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SSID = USB

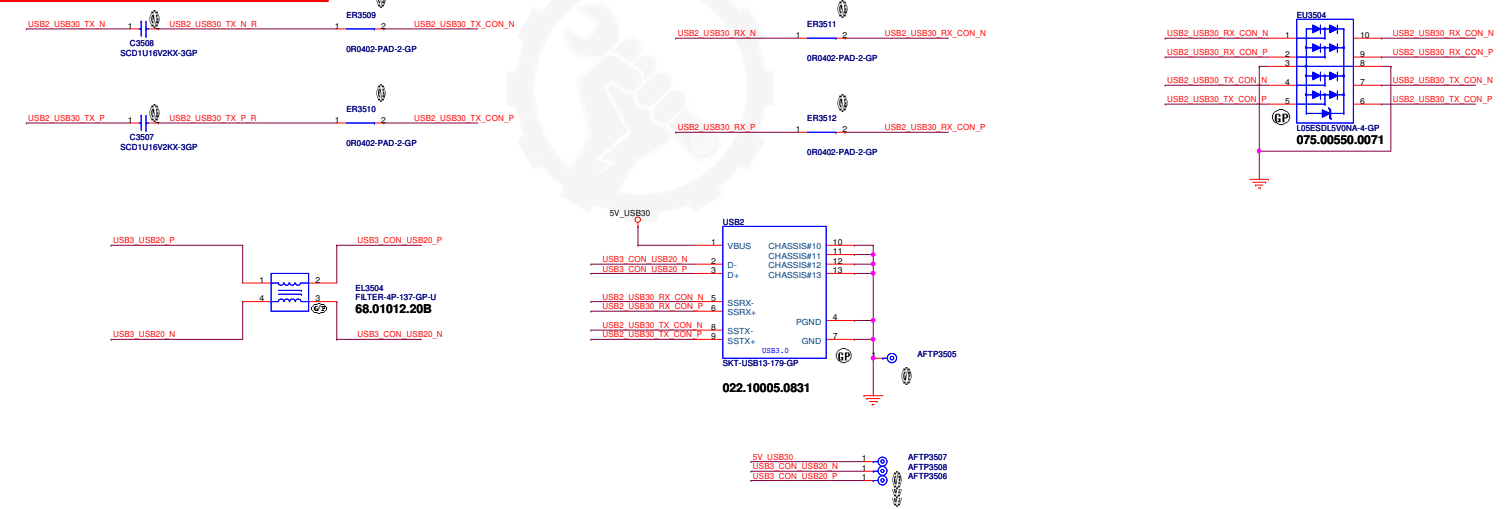
Main Func = USB3.0 Port1

[16] USB1_USB30_TX_N >>>
[16] USB1_USB30_TX_P >>>
[16] USB1_USB30_RX_N <<<
[16] USB1_USB30_RX_P <<<
[17] USB2_USB20_P <<<
[17] USB2_USB20_N <<<

[16] USB2_USB30_RX_N <<<
[16] USB2_USB30_RX_P <<<
[16] USB2_USB30_TX_N <<<
[16] USB2_USB30_TX_P <<<
[17] USB3_USB20_P <<<
[17] USB3_USB20_N <<<



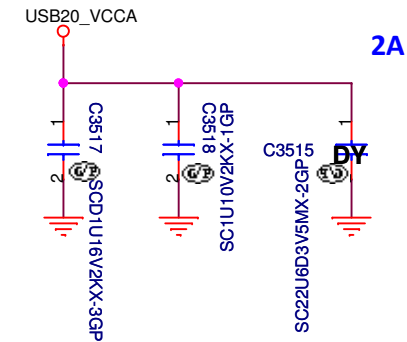
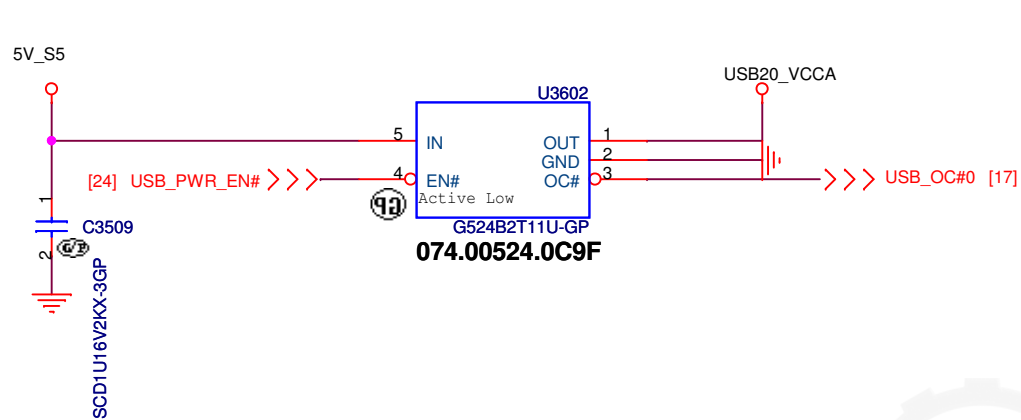
Main Func = USB3.0 Port2



Main Func = USB Power SW

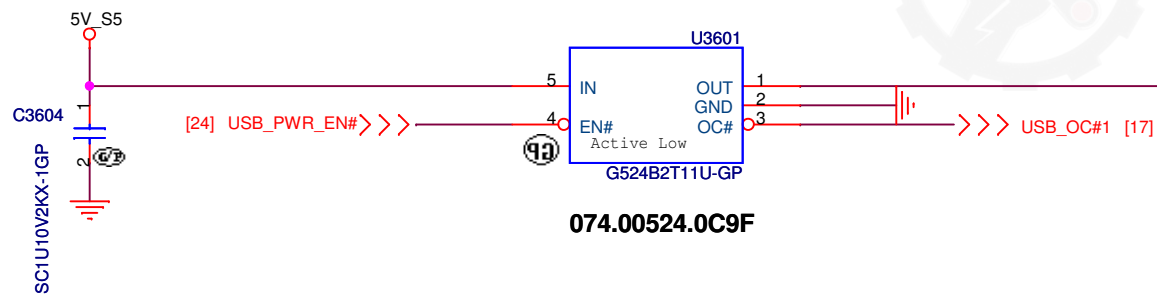
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USB2.0 Port3 (IO Board)

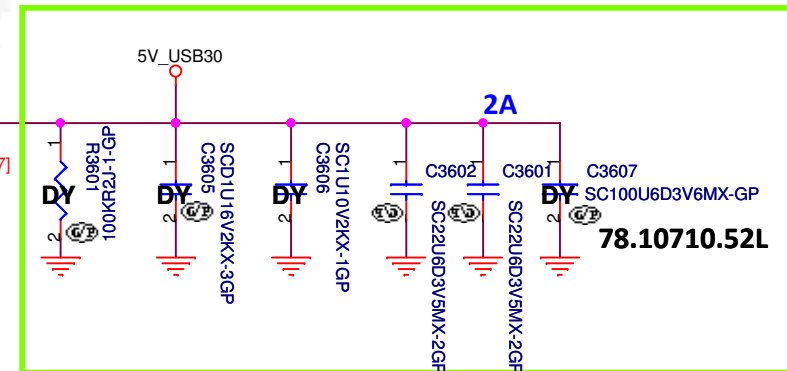


Layout Note: Close CON1

USB3.0 Port1



Layout Note: Close USB1



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Title				USB Power SW					
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USB2.0 HUB

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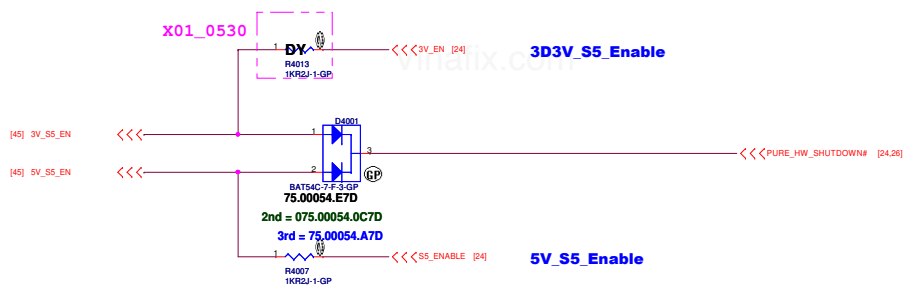


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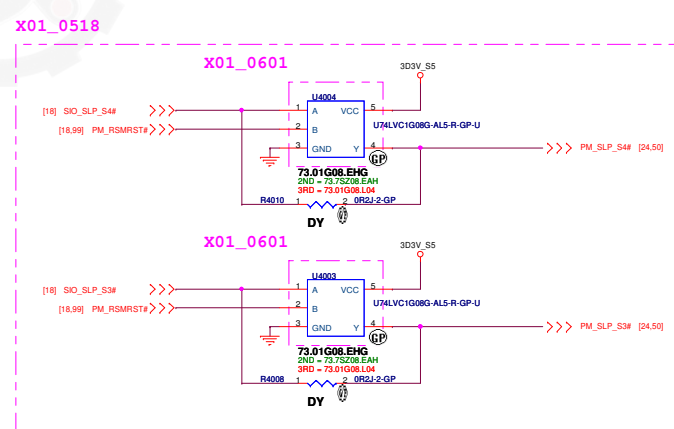
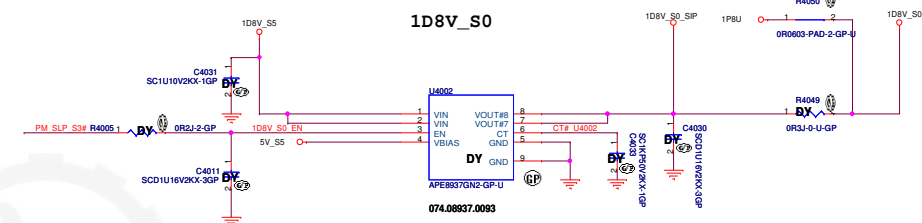
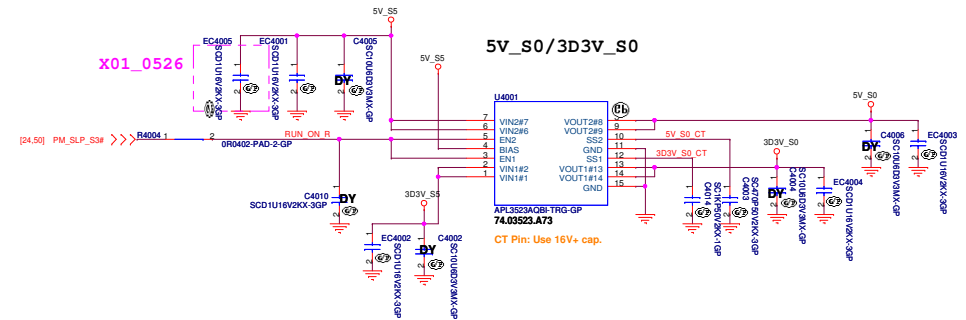
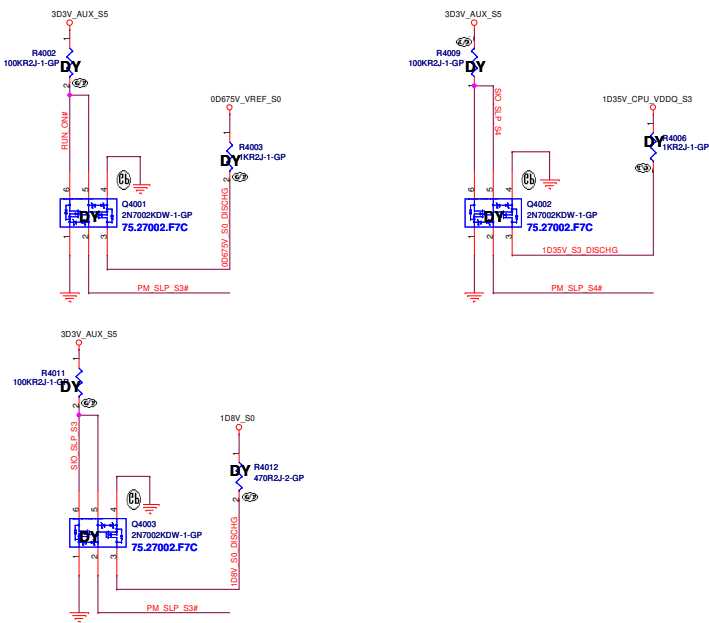
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SSID = Reset.Suspend

Power Sequence



Discharge circuit



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Size A4	Document Number Turis APL UMA	Rev X02
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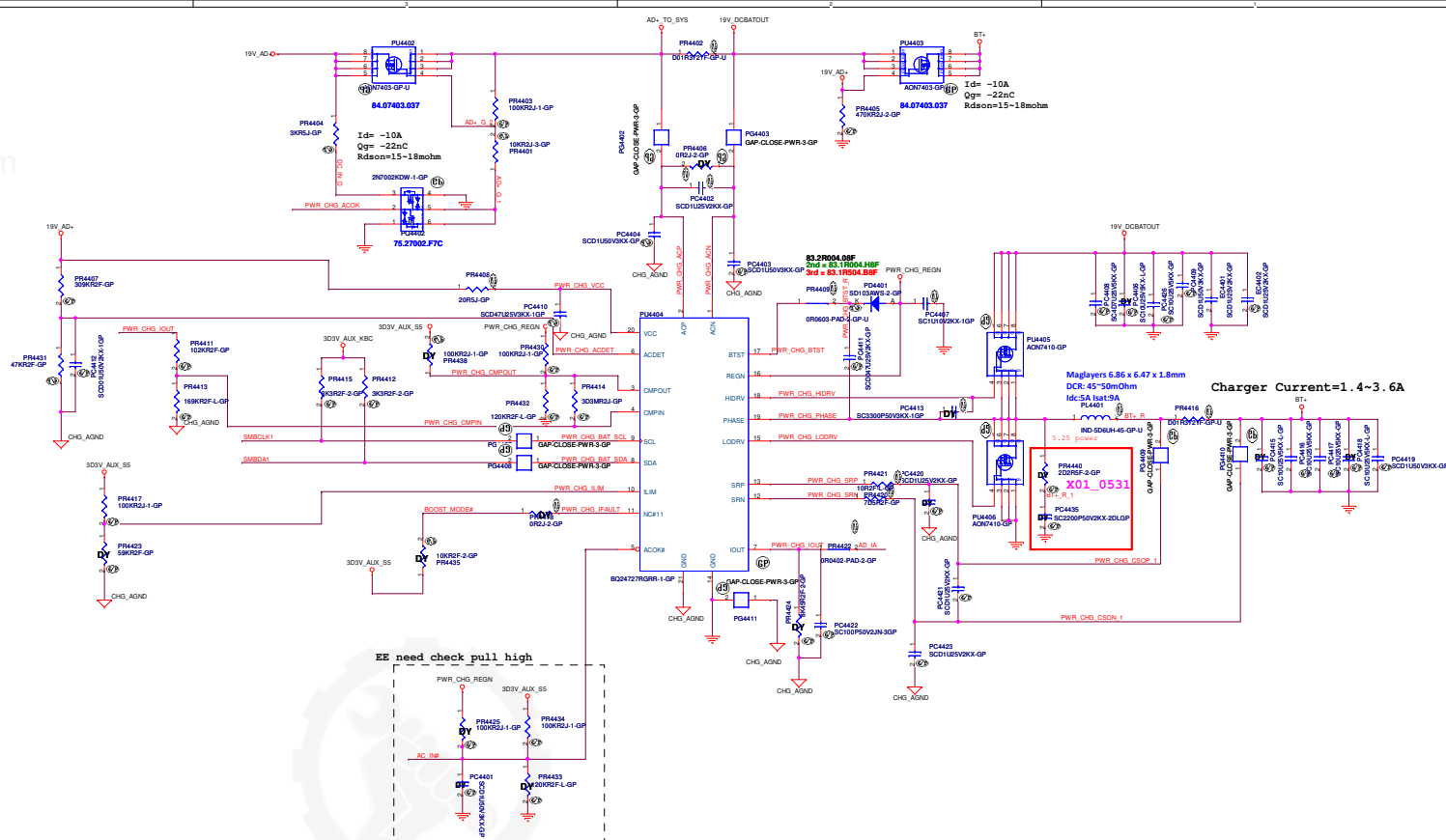
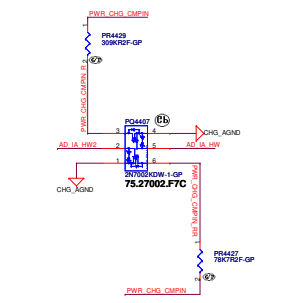
Date: Wednesday, July 27, 2016 Sheet 42 of 106

[D4] AD_IA_HW >>>
 [D4] AD_IA_HW2 >>>
 [D4-43] SBMCLK1 <<<
 [D4-43] SBMCLK1 <<<
 [D4] AC_IN <<<
 [D4-43] AD_IA <<<
 [D4-43] PRAT_PRESA >>>
 [18-24] H_PROCHOT <<<

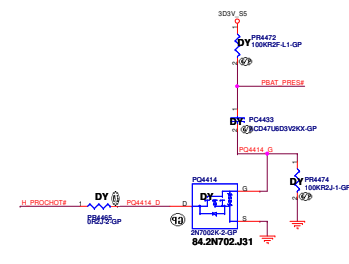
AD_IA_HW_SETTING

EC code only BQ24727

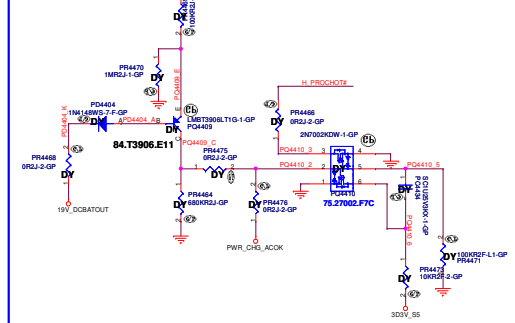
H_PROCHOT#	AD_IA_HW	AD_IA_HW2
35W	0	0
45W	1	0
65W	0	1



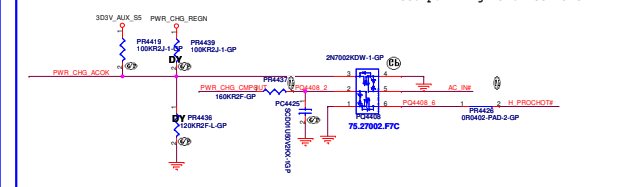
Battery PROCHOT# circuit



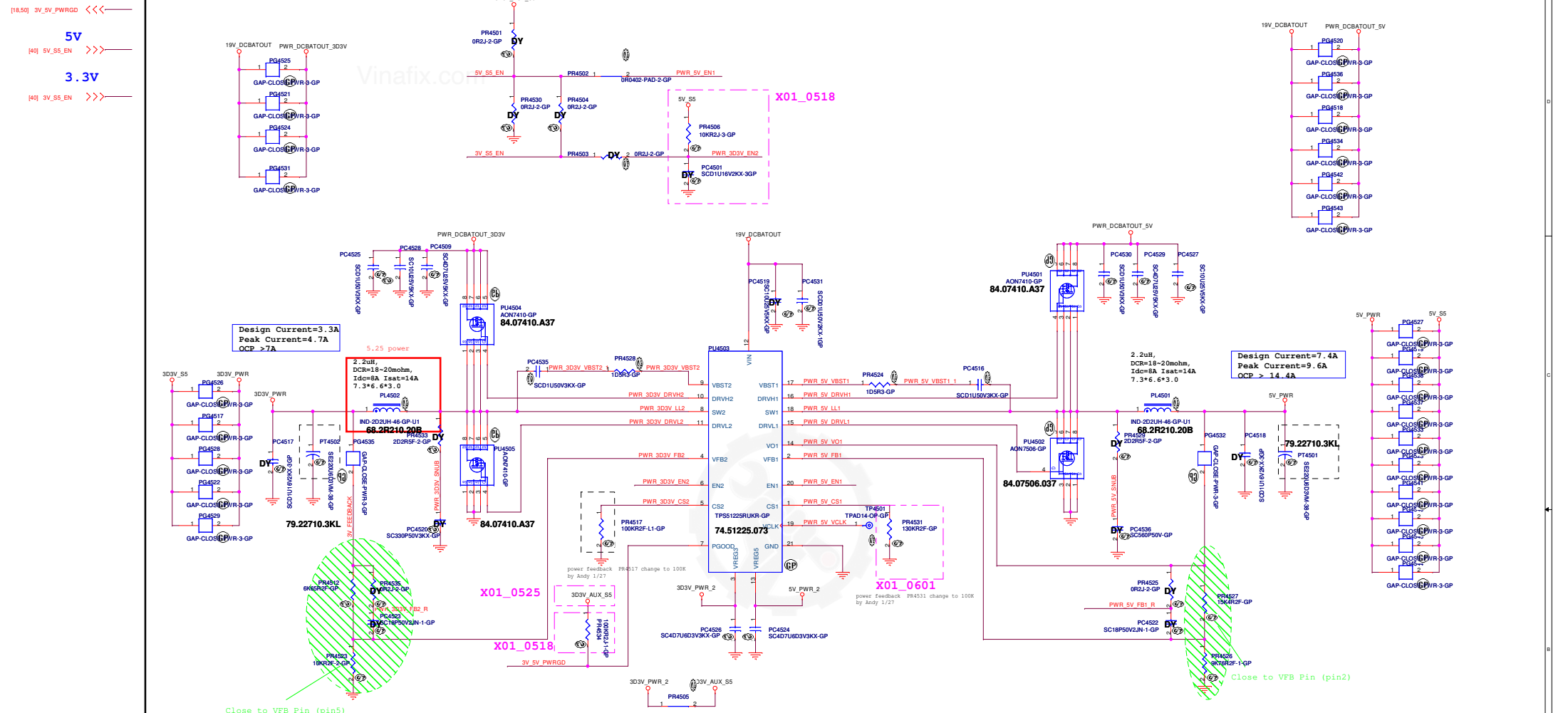
Adapter PROCHOT# circuit



EE need pull high and net name



Core Design



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037



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Title

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Size
A4

Document Number

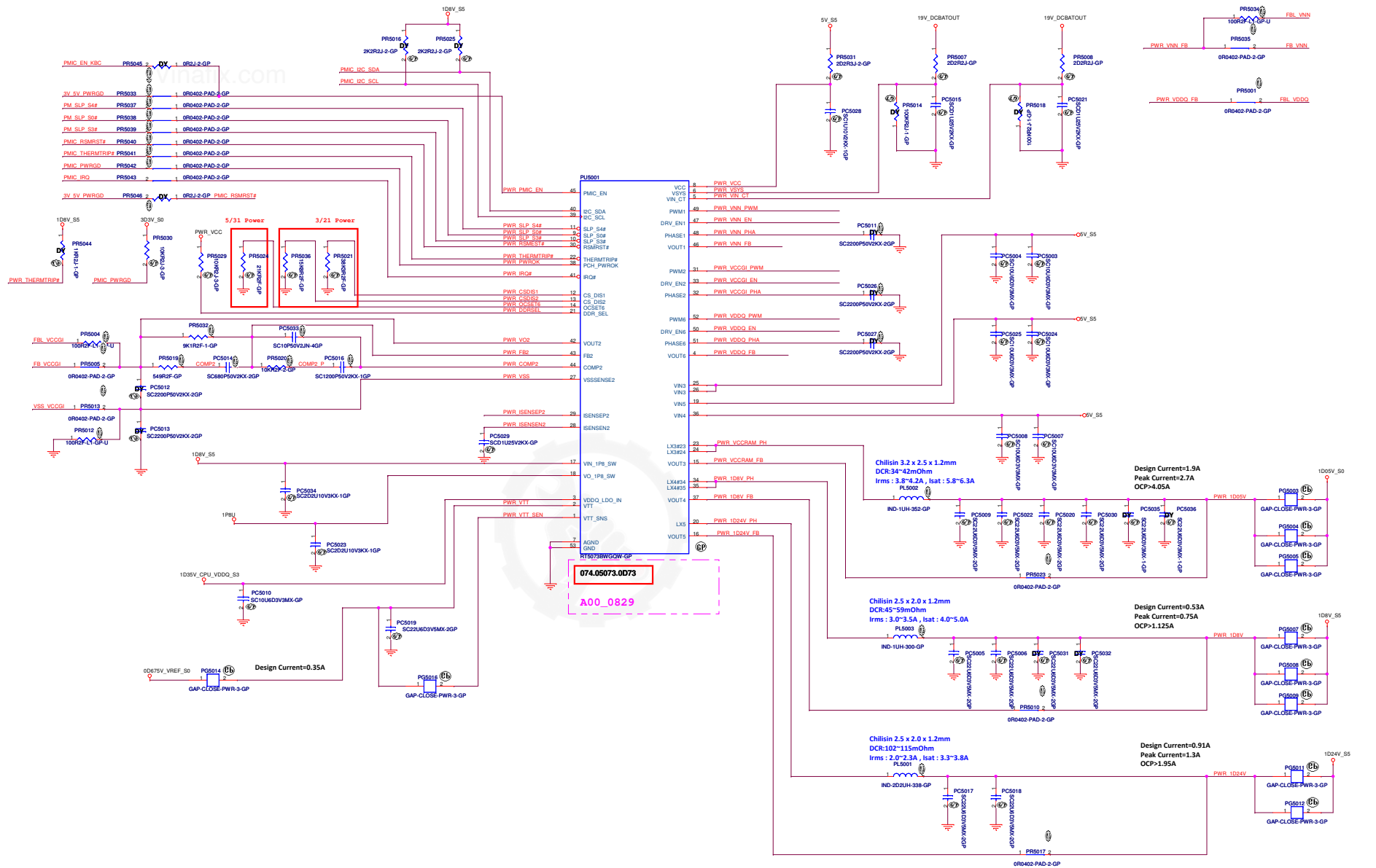
Turis APL UMA

Rev
X02

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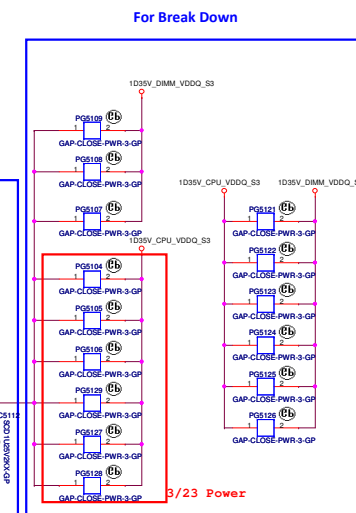
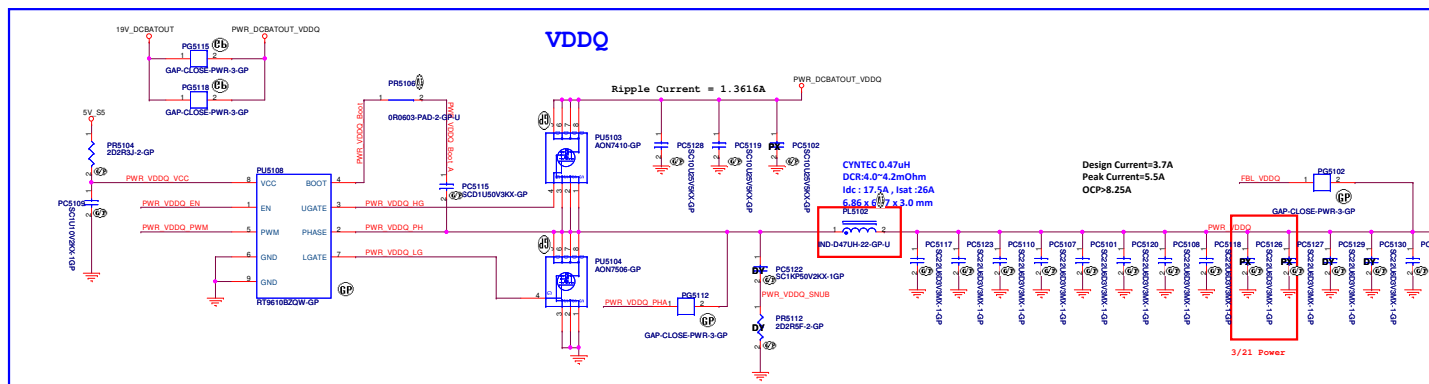
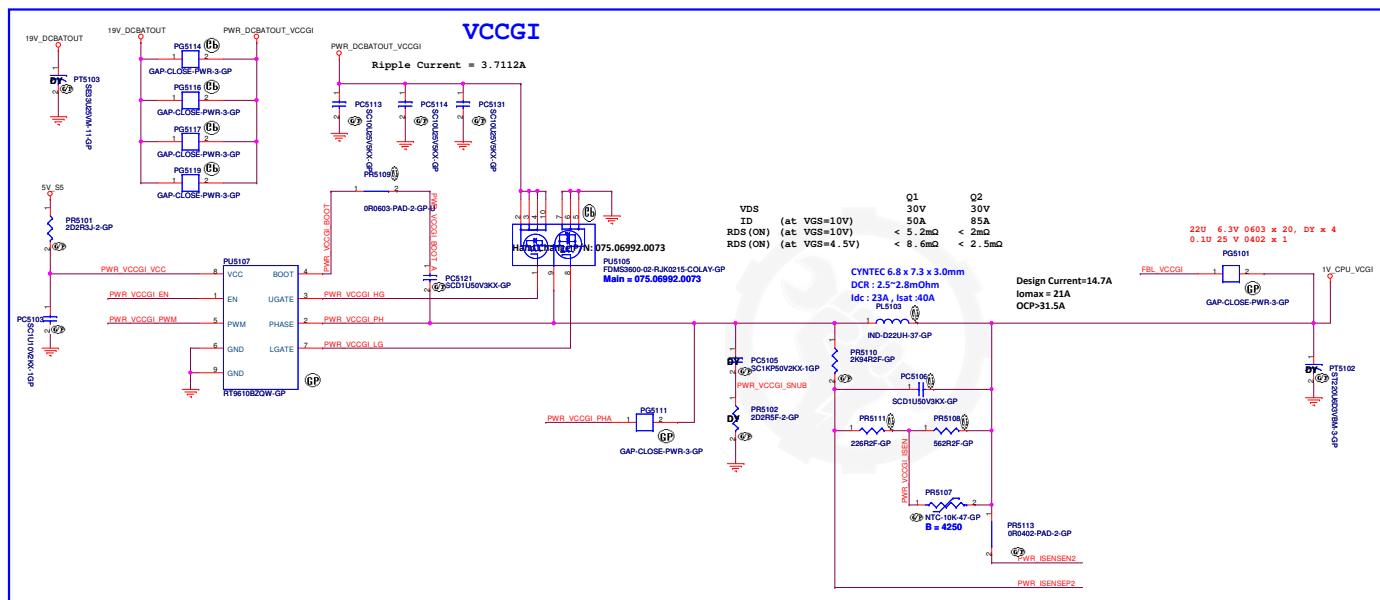
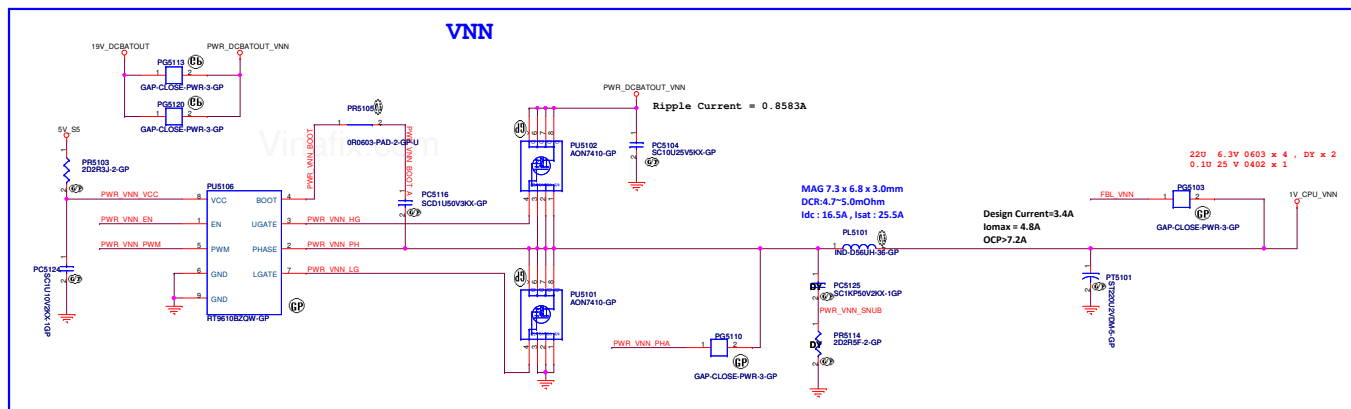
[16] PMIC_RC_SDA >>>
 [16] PMIC_RC_SCL >>>
 [18.40] 3V_SV_PWRGD >>>
 [18.24] PM_SLP_S4# >>>
 [18.24] PM_SLP_S0# >>>
 [18.24] PM_SLP_S3# >>>
 [18.24] PMIC_RSTMST# <<<
 [18.24] PMIC_THERMTRIP# <<<
 [20.24.26] PMIC_PWRGD <<<
 [24] PMIC_IRQ <<<
 [24] PMIC_EN_KBC >>>
VNN
 [51] PWR_VNN_EN <<<
 [51] PWR_VNN_PWM <<<
 [51] PWR_VNN_PHA >>>
 [51] PWR_VNN_FB >>>
 [5] FBL_VNN >>>
 [7] FB_VNN >>>
VCCGI
 [51] PWR_VCCGI_EN <<<
 [51] PWR_VCCGI_PWM <<<
 [51] PWR_VCCGI_PHA >>>
 [51] FBL_VCCGI >>>
 [7] FB_VCCGI >>>
 [7] VSS_VCCGI >>>
 [51] PWR_ISENSE2 <<<
 [51] PWR_ISENSE2 <<<
VDDQ
 [51] PWR_VDDQ_EN <<<
 [51] PWR_VDDQ_PWM <<<
 [51] PWR_VDDQ_PHA >>>
 [51] FBL_VDDQ >>>



```
[50] PWR_VNN_EN>>>
[50] PWR_VNN_PWM>>>
[50] PWR_VNN_PHA<<<
[50] FBL_VNN<<<
```

```
[50] PWR_VCCGI_EN >>> _____
[50] PWR_VCCGI_PWM >>> _____
[50] PWR_VCCGI_PHA <<< _____
[50] FBL_VCCGI <<< _____
[50] PWR_ISENSEN2 <<< _____
[50] PWR_ISENSE2 <<< _____
```

```
[50] PWR_VDDQ_EN >>> _____
[50] PWR_VDDQ_PWM >>> _____
[50] PWR_VDDQ_PHA <<< _____
[50] FBL_VDDQ <<< _____
```



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File			
PMIC (2)			
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SSID = PWR.Plane.Regulator_1p8v

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Title <Title>		
Size A3	Document Number Turis APL UMA	Rev X02
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Main Func = 1D05V

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Title			<Title>	
Size	Document Number			Rev
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Main Func = 1D24V

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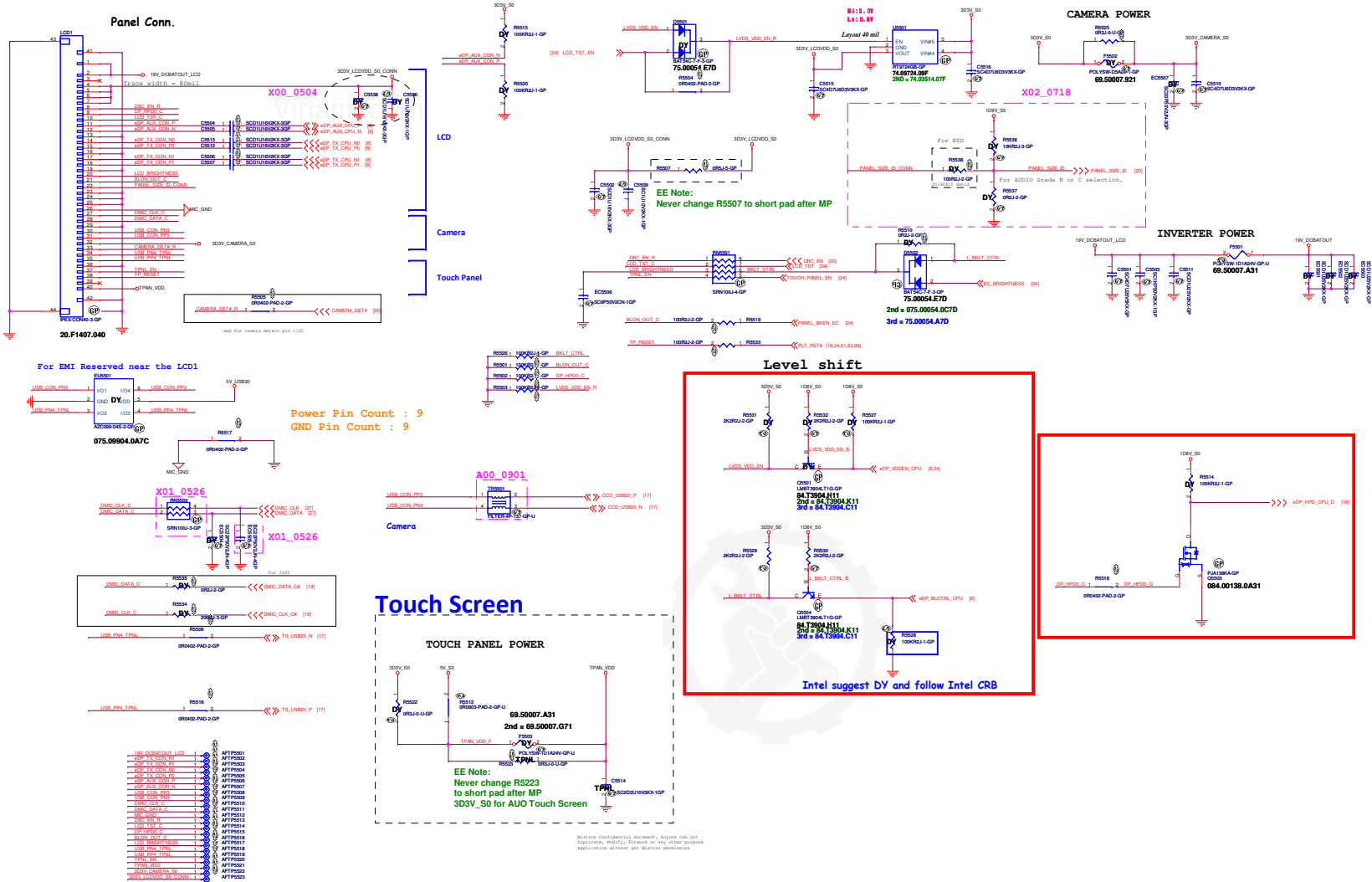


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Title			<Title>	
Size	Document Number			Rev
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Main Func = CRT

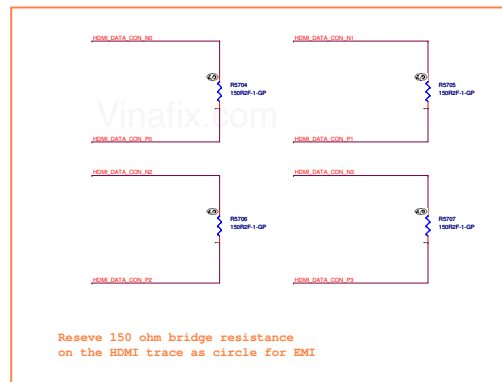
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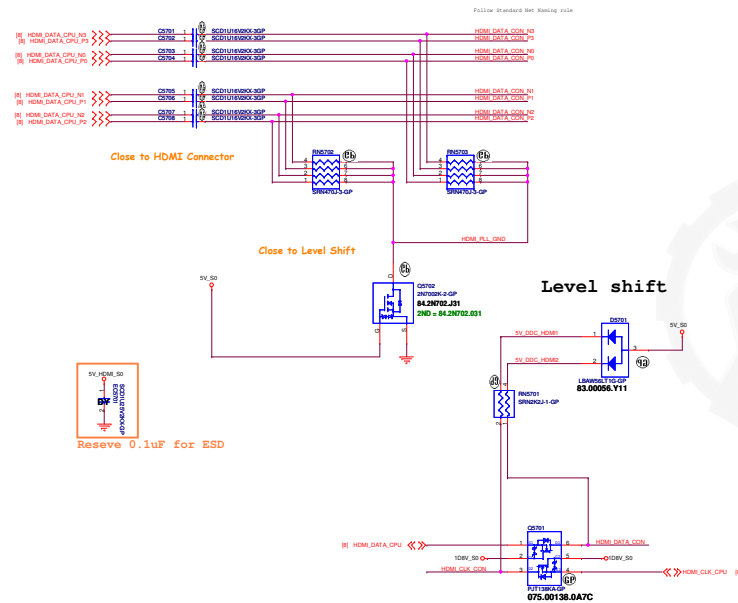


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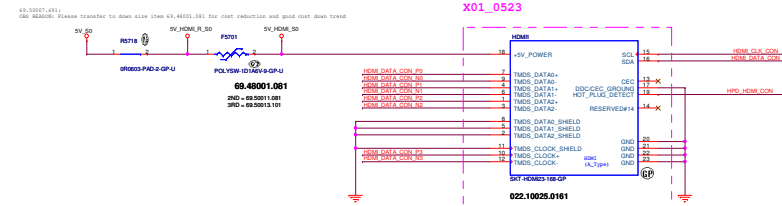
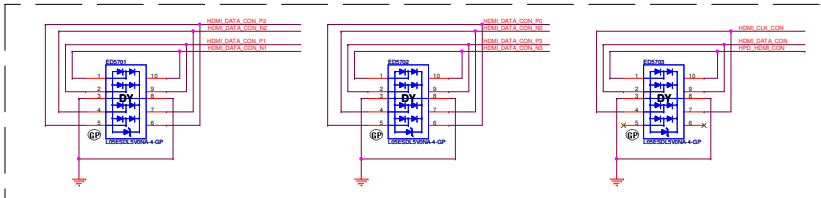
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT			
Size A4	Document Number Turis APL UMA		Rev X02
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HDMI Level Shifter & CONNECTOR



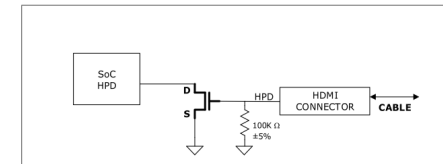
EMI Request:



14.3.5 HDMI HPD Implementation

The hot-plug detect output from HDMI sink device is a 5/3.3V active high signal. Since the input on the processor is a 1.8V active low signal, a logic inversion circuit is required on the motherboard. Figure 173 shows an example of this implementation.

Figure 173. HDMI HPD Passgate Design Recommendation




NOTES:

- It is highly recommended that the passgate N-MOSFET device selected has Gate Threshold Voltage $<= 1.5V$
- It is required to enable internal 20K pull up resistor on the HV_DDIx_HPDI signals by BIOS

(Blanking)



<Core Design>

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SSID = DVI

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Title

(Reserved) DVI

Size

Document Number

Turis APL UMA

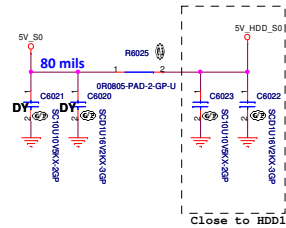
Rev

X02

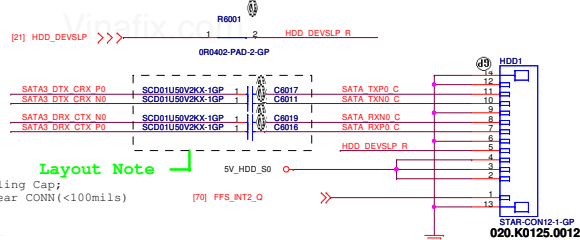
Date: Wednesday, July 27, 2016

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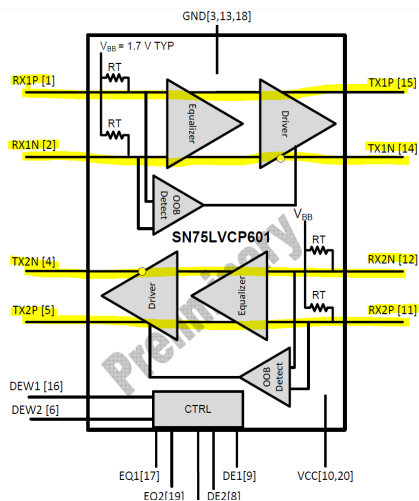
Main Func = HDD



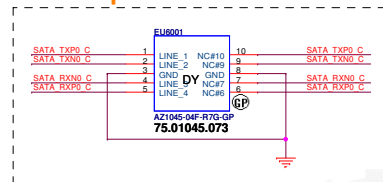
SATA HDD Connector



HDD Re-driver SN75LVCP601RTJR-GP



EMI Request



NON HDD Re-driver

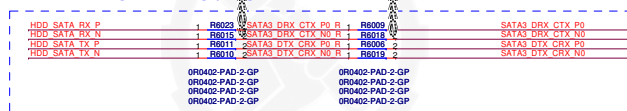


Table 1: Tx/Rx EQ & DE Pulse Width Settings

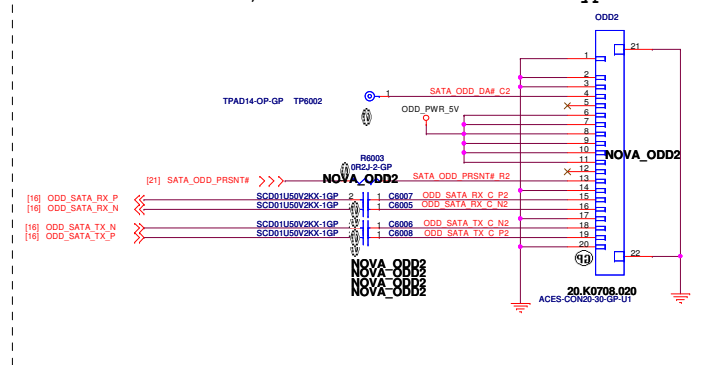
DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14

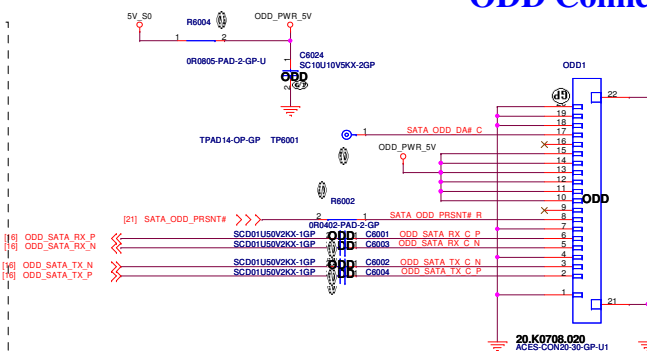
DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

Main Func = ODD

For NOVA if use ODD2, the cable need to add ont type



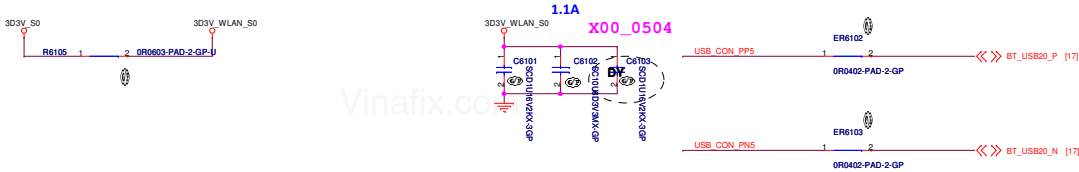
ODD Connector



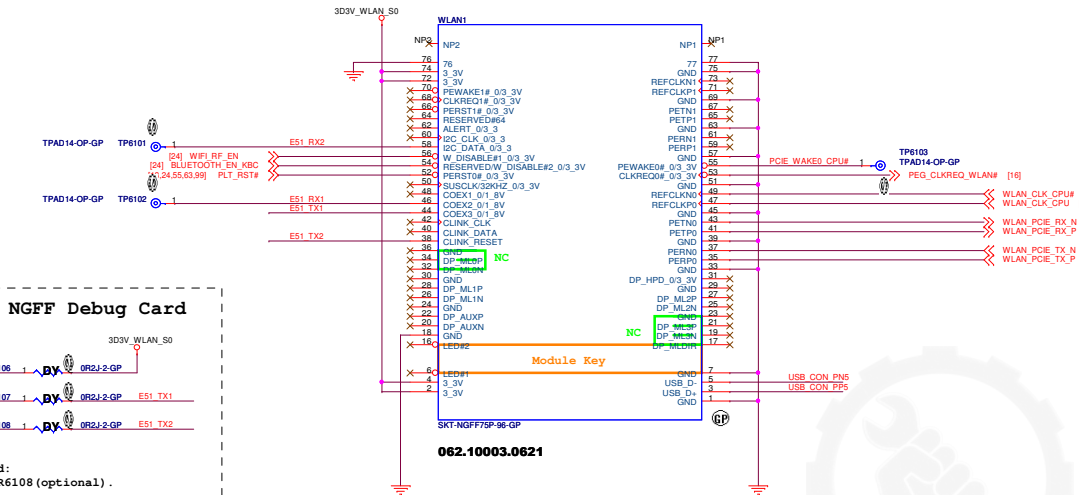
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SSID = WLAN

Mini Card Connector(802.11a/b/g)

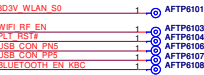


Note:pin 76 and pin 77 need contact to GND



Reserved for NGFF Debug Card

EE Note:
For NGFF Debug Card:
Stuff R6106, R6107, R6108 (optional).
DY R6105




SSID = WWAN

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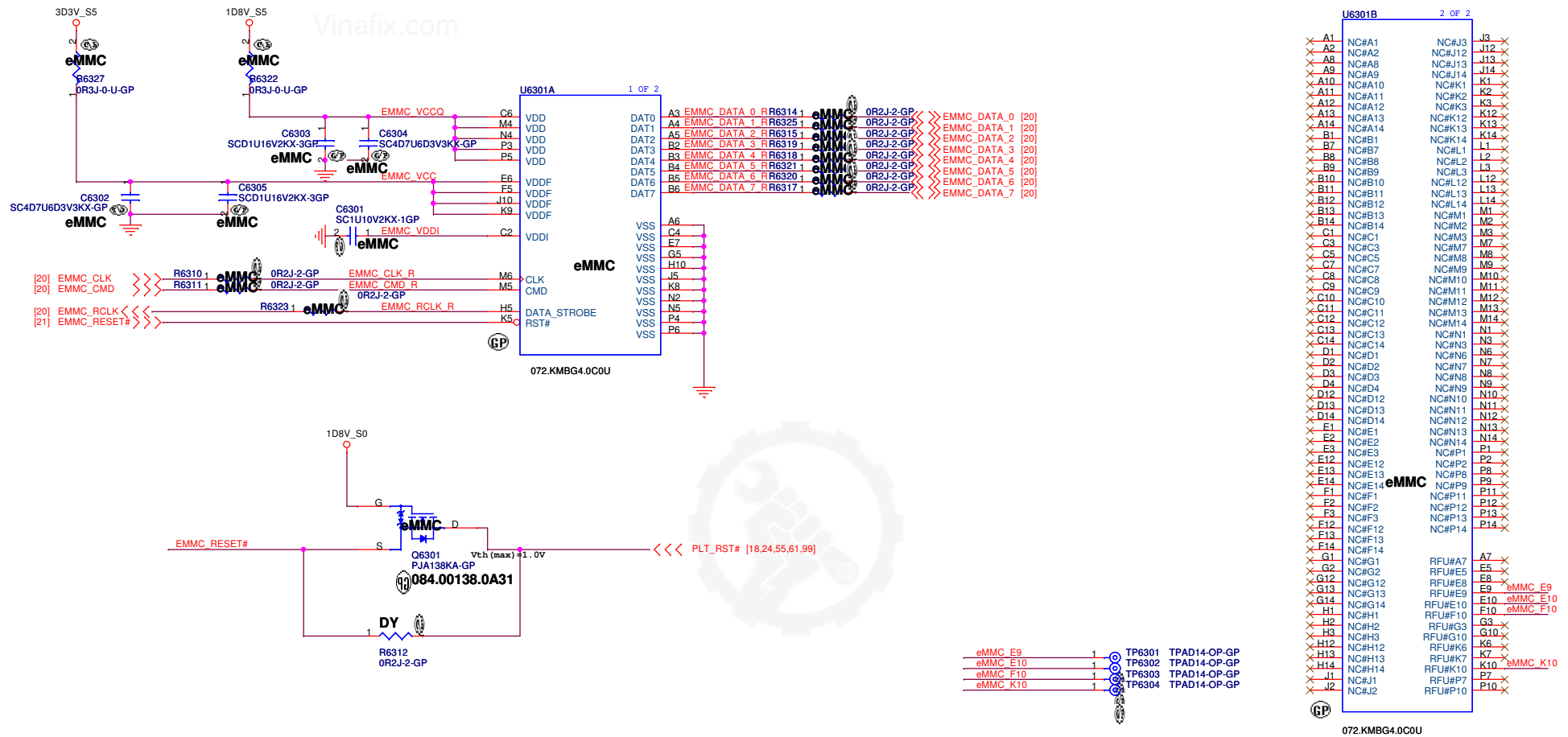
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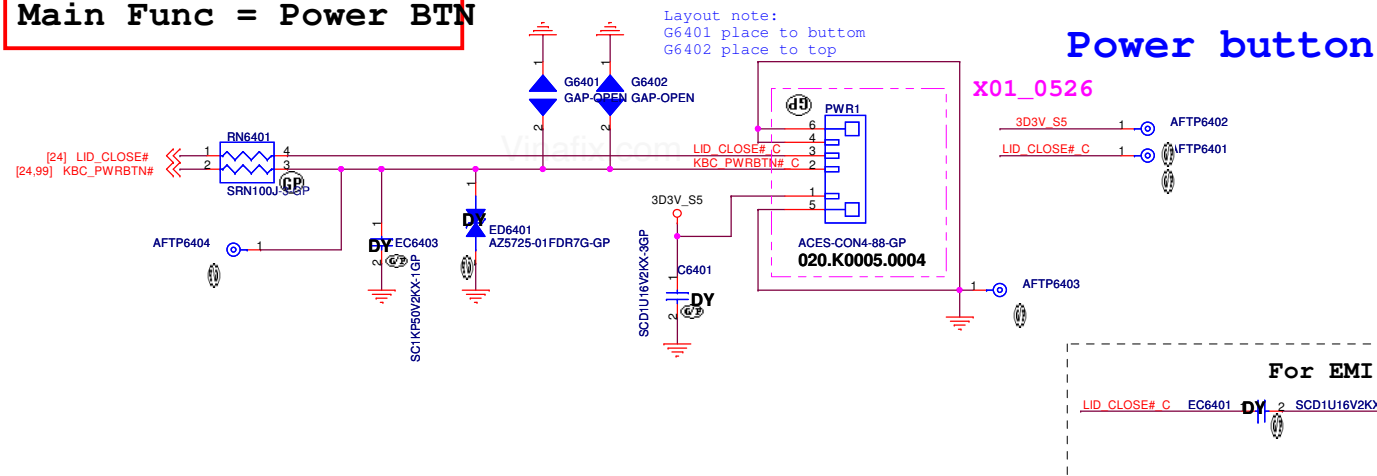
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved) WWAN			
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SSID = SSD-NGFF

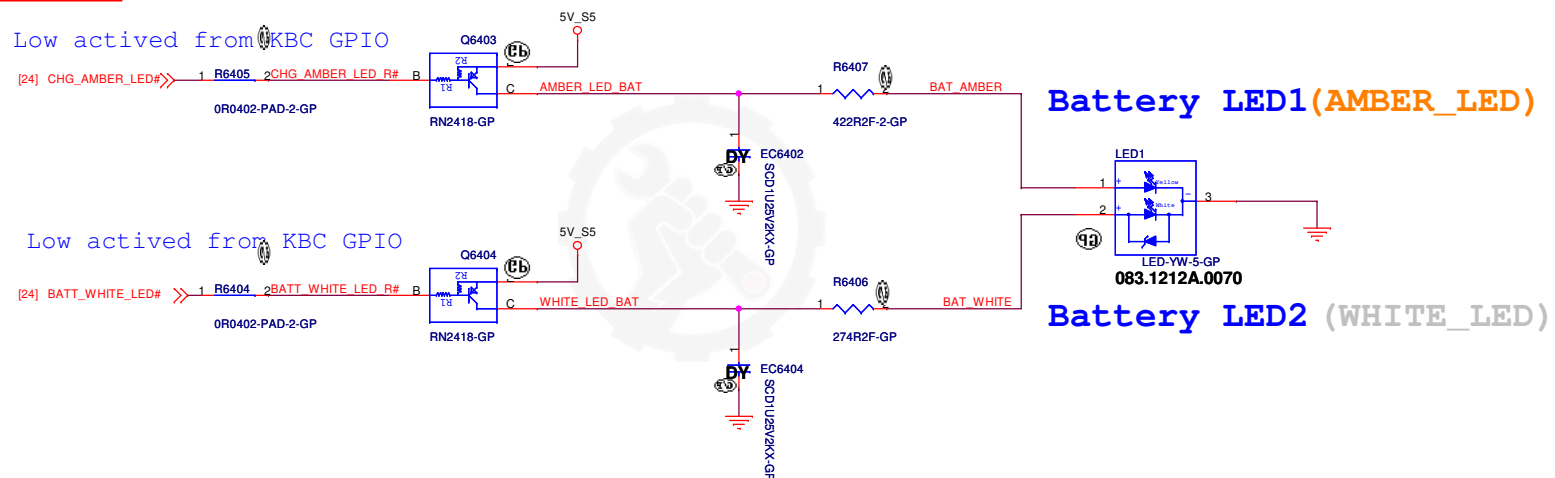


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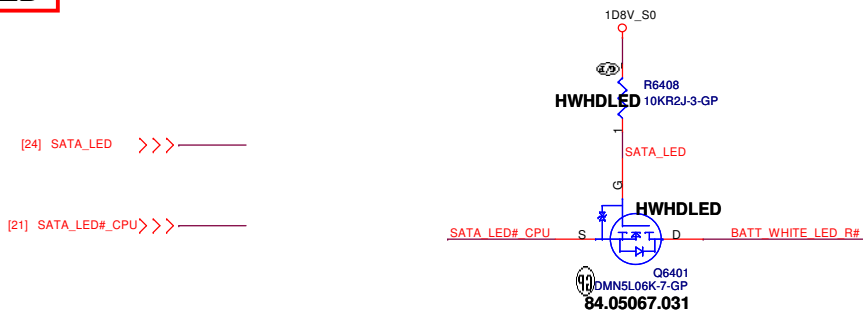
Main Func = Power BTN



Main Func = Battery LED



Main Func = HDD LED



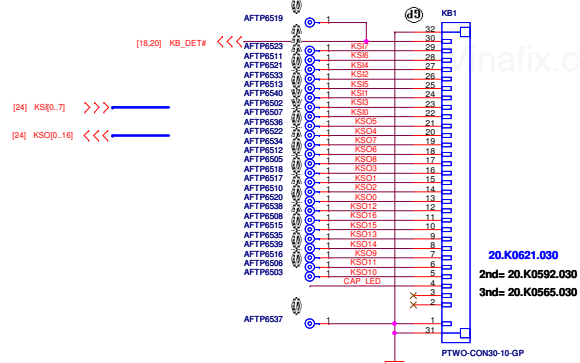
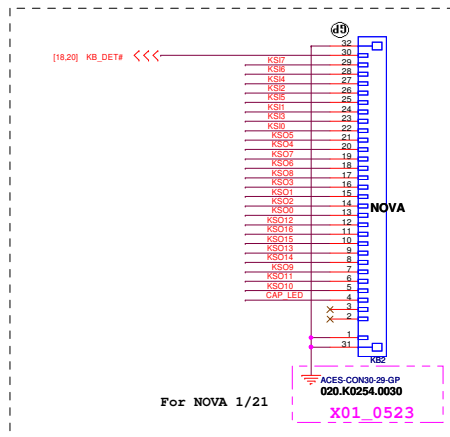
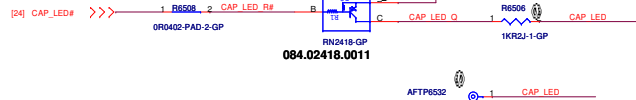
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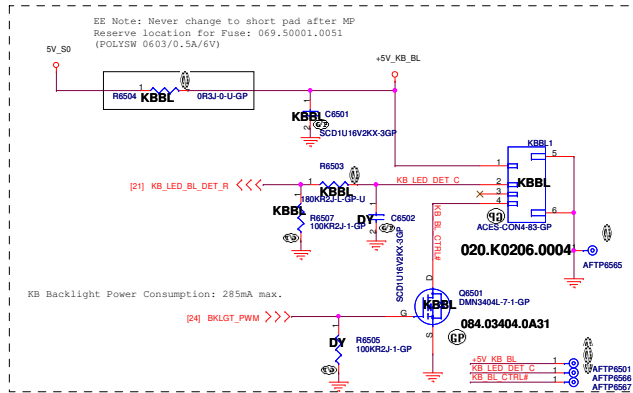
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Title		LED Board&Power Button	
Size	Document Number	Rev	
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Internal Keyboard Connector

CAP LED Control
LOW acted from KBC GPIO

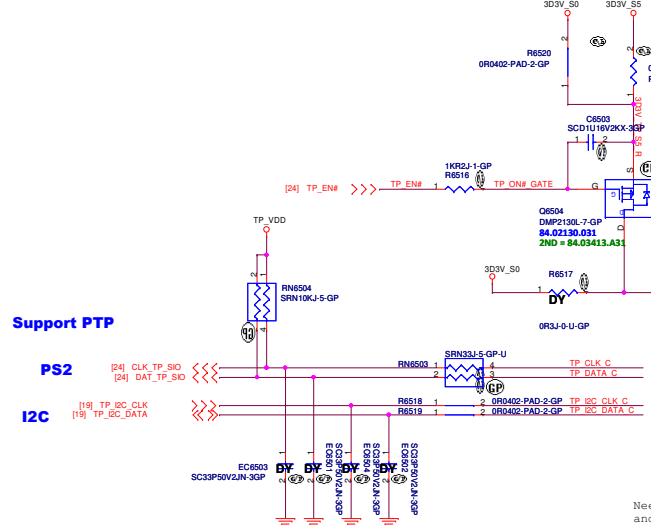
Keyboard Backlight (Reserved)



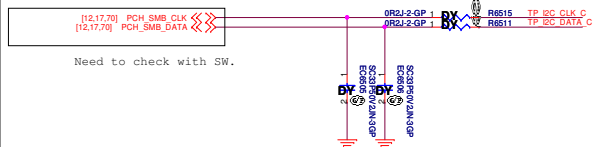
Support PTP

PS2

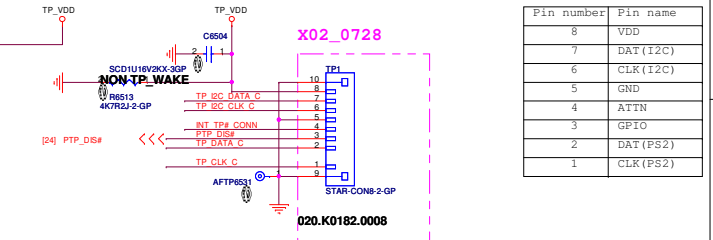
I2C



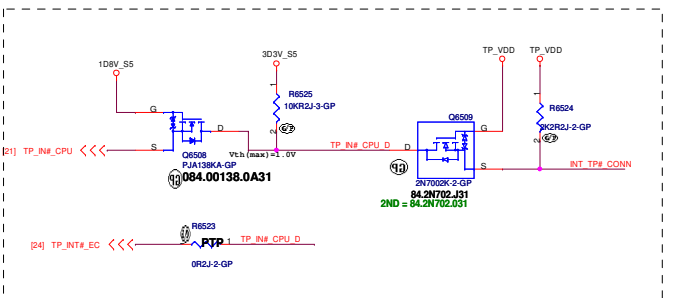
SMBUS



Precision Touch Pad Connector



INT#



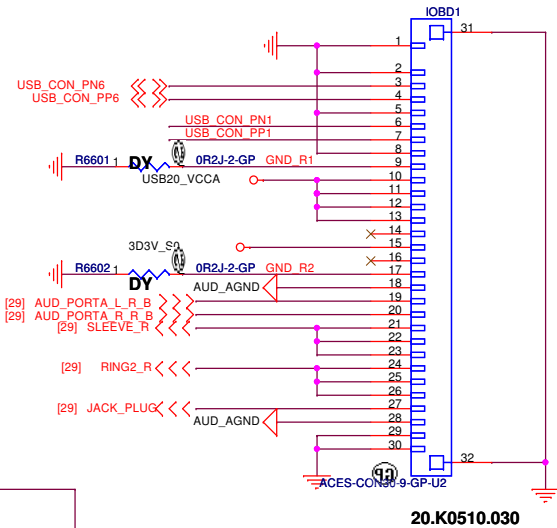
-Core Design-

Main Func = IO Connector

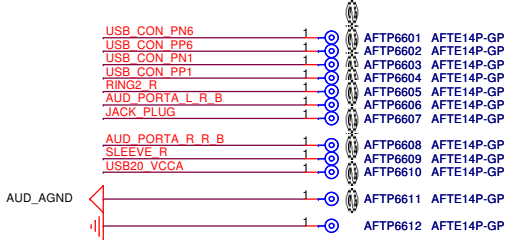
I/O Board Connector

Cardreader
USB3(USB2.0)

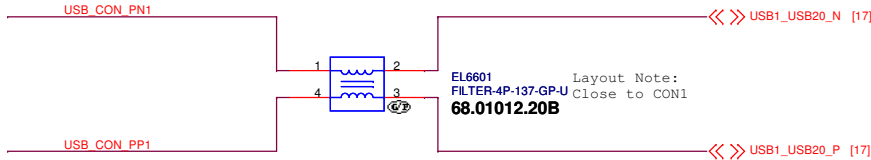
Universal Jack



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins

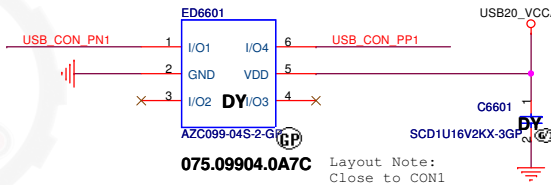


USB2.0 Port 1 CMC

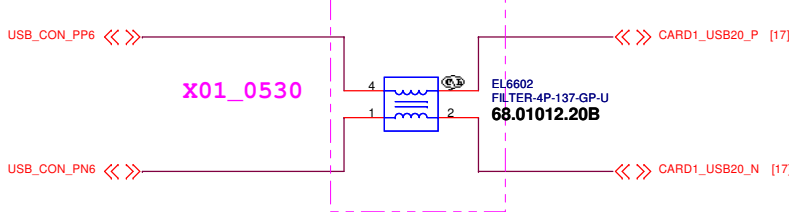


USB ESD Diode

Stuff for ESD R2 spec



Cardreader CMC



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Title

IO Board Connector

Size
A3

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SSID = User.interface

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Title

Hall Sensor

Size
A3

Document Number
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SSID = Debug CONN

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Title

(Reserved) Debug CONN

Size
A4

Document Number

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SSID = Sensor

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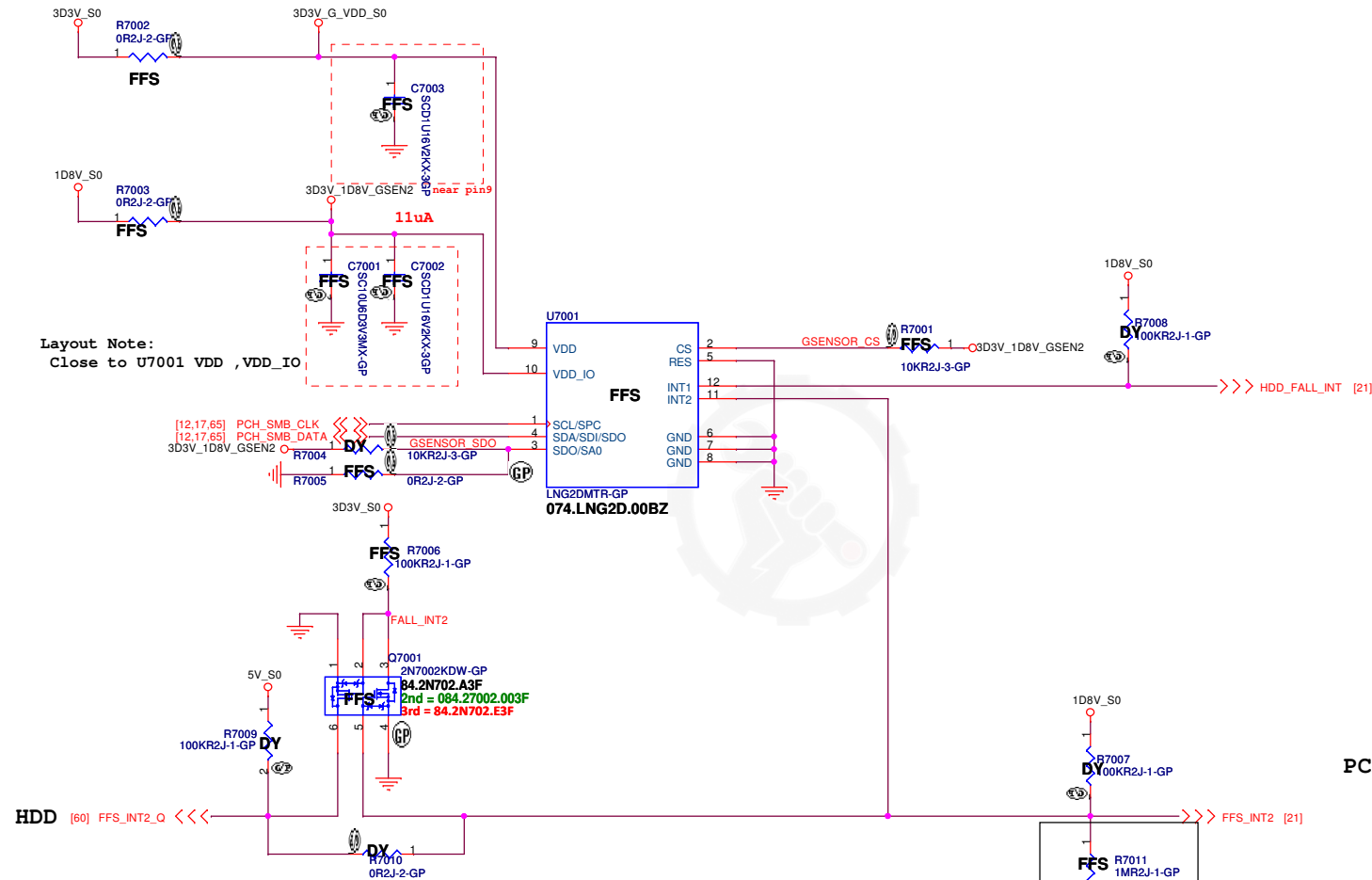


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Title			
Hall Sensor			
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Free Fall Sensor

DVT1 add FFS 2/18



Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

2014.04.24 Venrer suggest, reserve to prevent error trigger

<Core Design>




Title			Free Fall Sensor		
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<Core Design>

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Title (Reserved)Thunderbolt (1/5)		
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<Core Design>

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Title <i>(Reserved)Thunderbolt (2/5)</i>			
Size A4	Document Number <i>Turis APL UMA</i>		Rev <i>X02</i>
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Title (Reserved)Thunderbolt (3/5)		
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Title <i>(Reserved)Thunderbolt (4/5)</i>			
Size A4	Document Number <i>Turis APL UMA</i>		Rev <i>X02</i>
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Title (Reserved)Thunderbolt (5/5)		
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Main Func = dGPU

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Title			GPU(1/5) PEG		
Size	Document Number				Rev
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Main Func = dGPU

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Title GPU (2/5) DIGITALOUT			
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Title			GPU (3/5) VRAM I/F		
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Main Func = dGPU

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Title			GPU (4/5) GPIO/STRAP		
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Main Func = dGPU

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Title			GPU (5/5) PWR/GND		
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Main Func = Vram (DDR3L)

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Title

GPU-VRAM1,2 (1/4)

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Main Func = Vram (DDR3L)

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Title GPU-VRAM3,4 (2/4)			
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Title

GPU-VRAM5,6 (3/4)

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Title

GPU-VRAM7,8 (4/4)

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Title

GPU CORE ISL62771HRTZ

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Title

GPU Discrete Power

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Title

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Size
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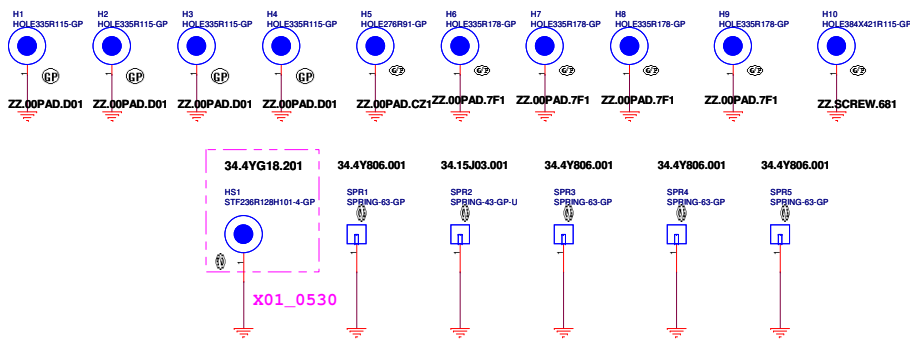


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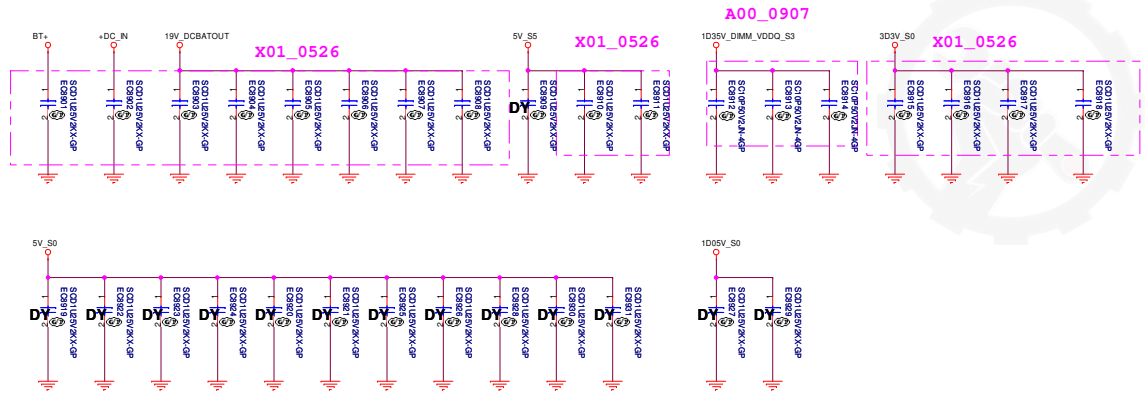
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Main Func = Unused Parts

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Main Func = EMI Capacitors



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Title (Reserved)NFC Connector			
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Title

(Reserved) TPM

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Title			(Reserved)Finger Print		
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Title			
(Reserved)Express Card			
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Title <i>(Reserved)Smart Card Socket</i>			
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Title (Reserved)SW GFX eDP			
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Title

(Reserved)Bottom Docking

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Title			(Reserved)LAN		
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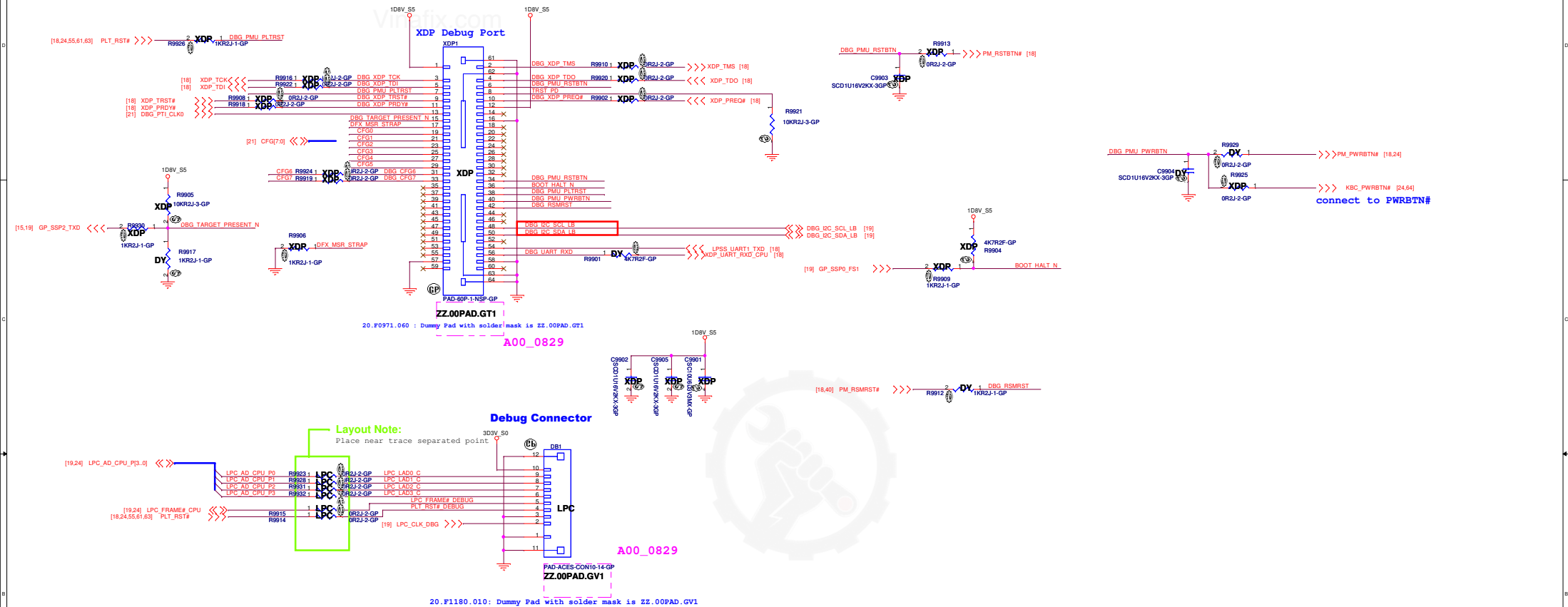


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Title **(Reserved)LAN SWITCH**

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SSID = DEBUG PORT



Processor Strapping

Table 2-36. Hardware Straps

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_36	VCC_1P24V_1P35V_A voltage selection	20K PD	1 = 1.35V 0 = 1.24V (default) Note: This strap will only be used for B-step. For A-step this rails should only be set at 1.24V
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) Note: Apollo Lake supports TXE3.0 (this is also called CSE) Note: This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_43	Allow eMMC as a boot source	20K PU	1=enable (default) 0=disable
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) Note: DnX: Download and Execute Note: This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_104	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_111	Boot BIOS Strap (BBS)	20K PU	1 = Do not boot from SPI (default) 0 = Boot from SPI
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override Note: This strap enables the platform to override security features in the SPI.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_117	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

Note: All the straps are sampled at Rising Edge of RSM_RST_N

GPIO_48	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) Note: Platforms should strap this LOW. Functionality is handled by the PMC.

USB2.0 MCP Side

Pair	Device
0	USB 2.0 port 1
1	USB 3.0 port 2
2	USB 3.0 port 3
3	Camera
4	Touch Panel
5	BT
6	Card Reader
7	N/A

USB3.0 MCP Side

Pair	Device
0	USB 3.0 port 2
1	USB 3.0 port 3
2	N/A
3	N/A
4	N/A


PCIE Table

PCIE	
Lane	Device
0	WLAN
1	N/A
2	N/A
3	N/A
4	N/A
5	N/A

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD

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Title			
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Change History-01

Size

Document Number

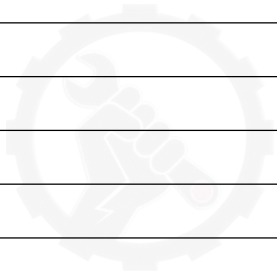
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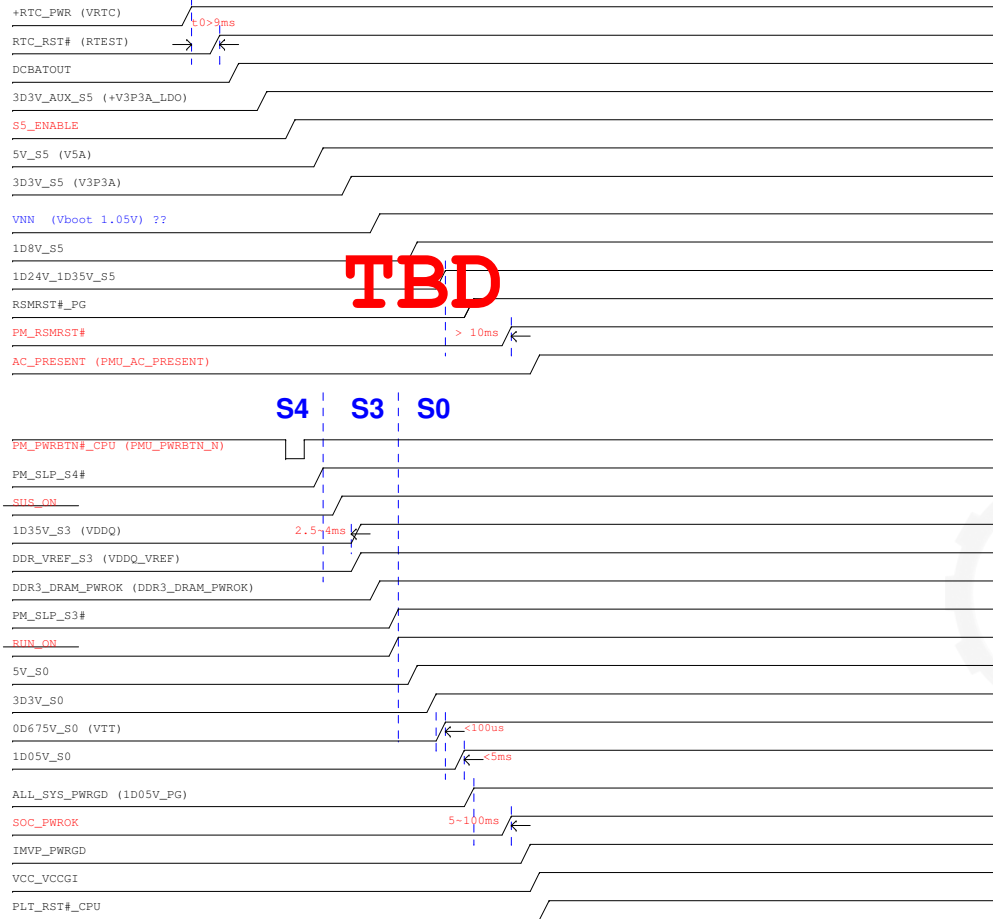
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Intel-Power Up Sequence

G3 to S5/S4

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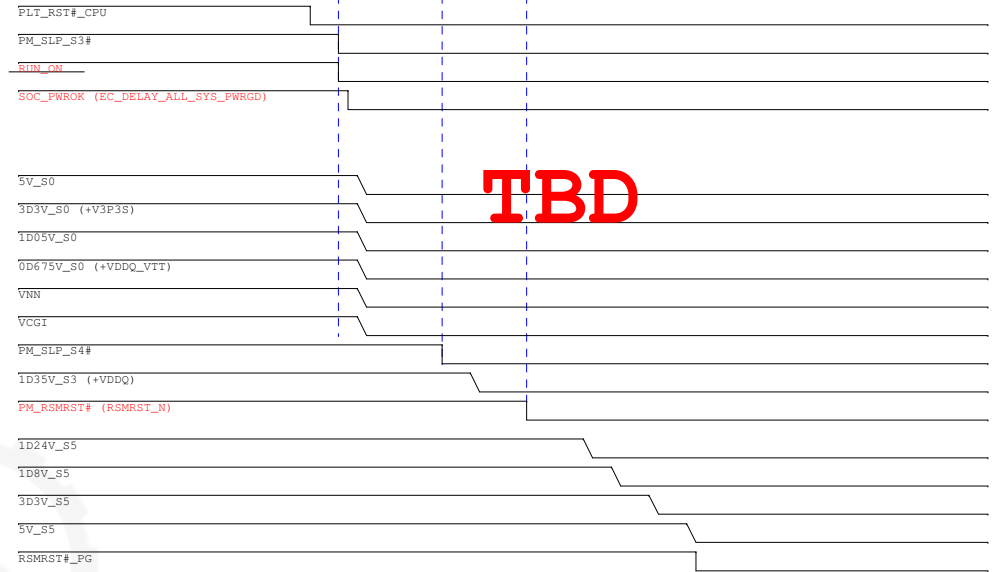
Red word : KBC GPIO



Intel-Power Down Sequence

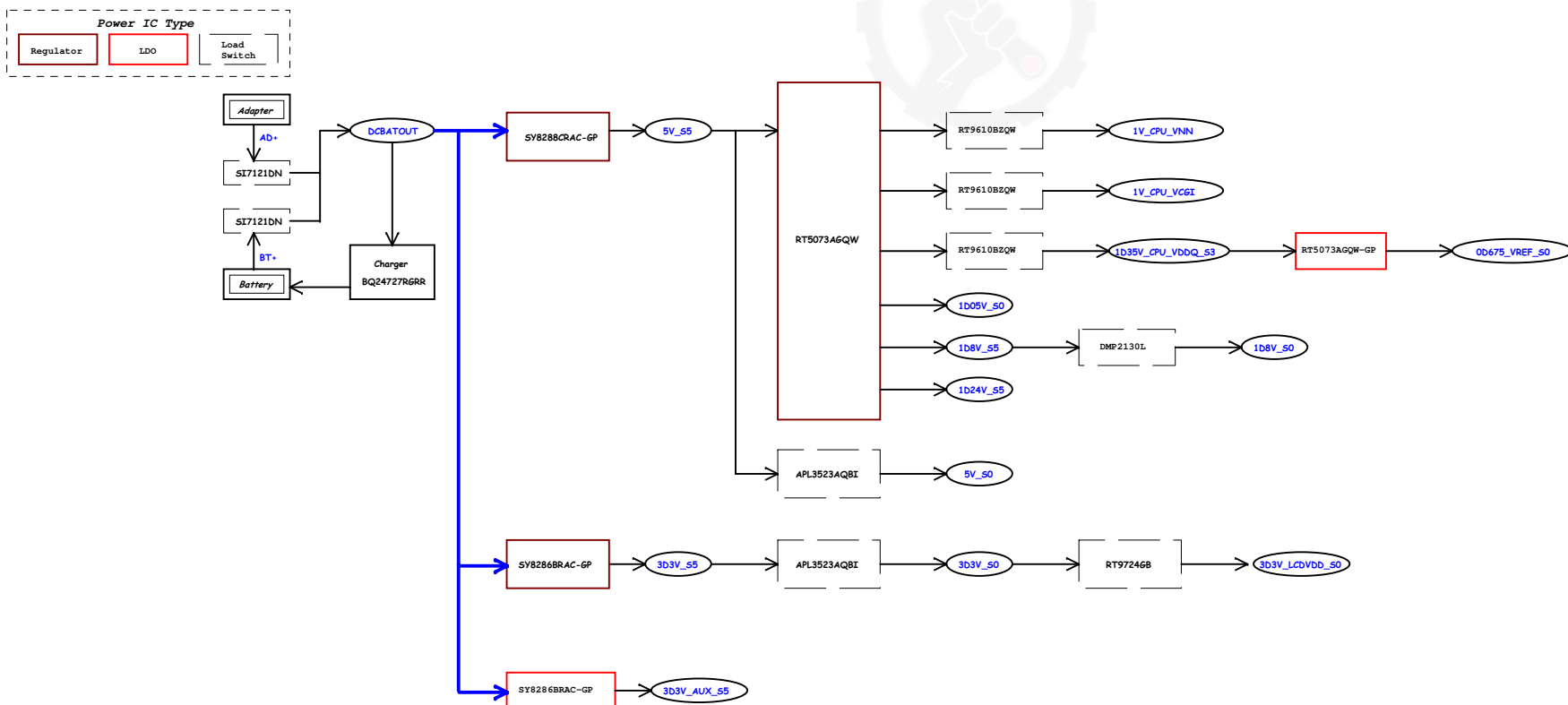
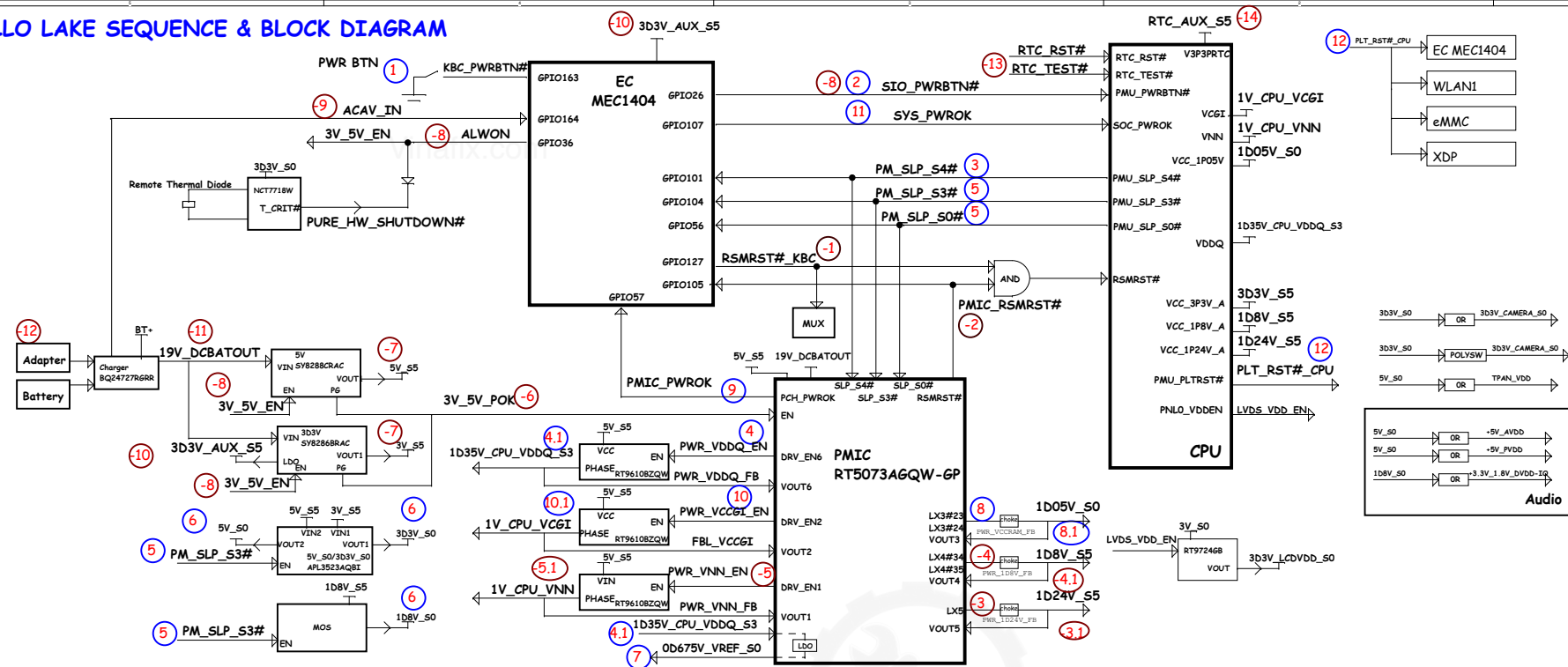
S0 S3 S4 G3

Red word : KBC GPIO



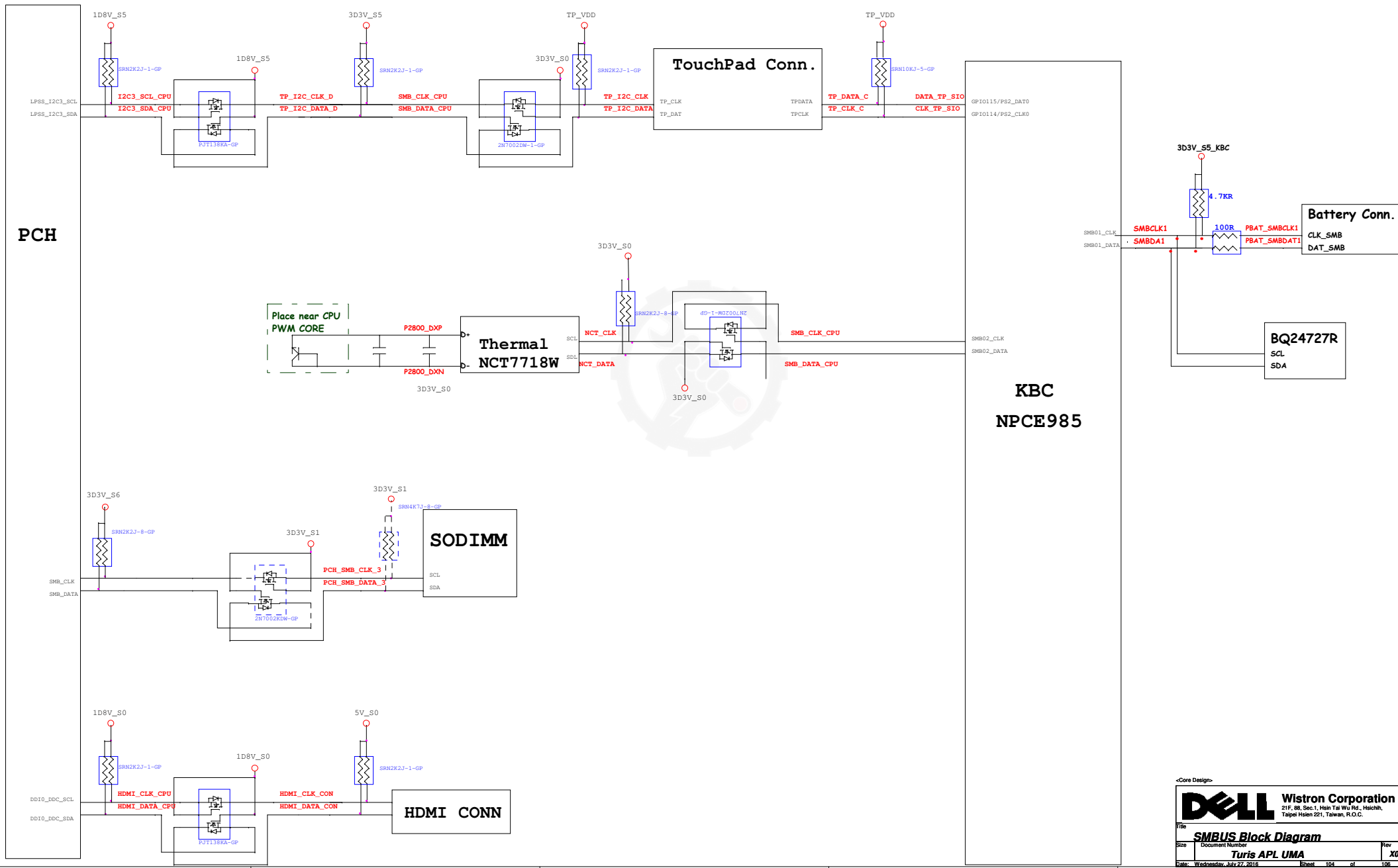
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APOLLO LAKE SEQUENCE & BLOCK DIAGRAM



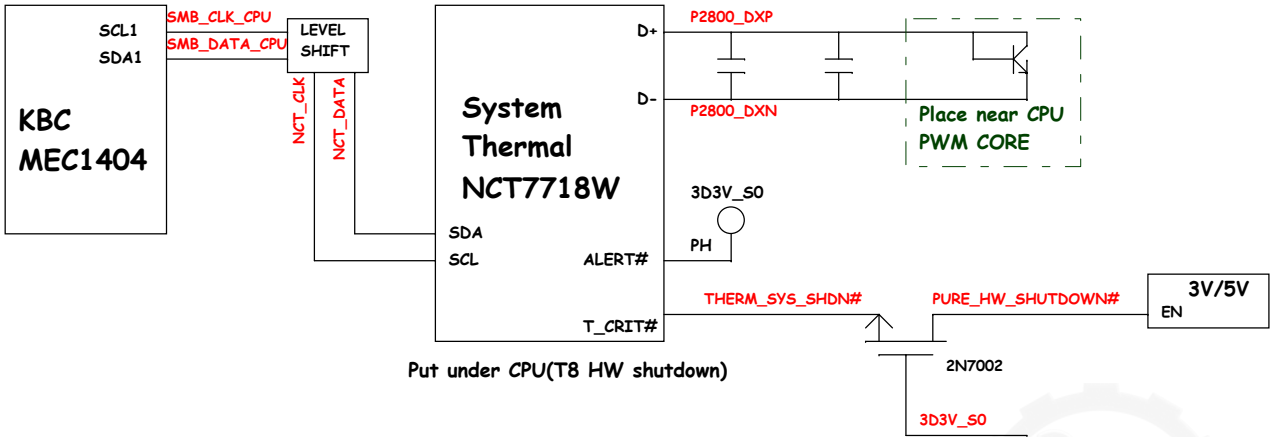
SMBus Block Diagram

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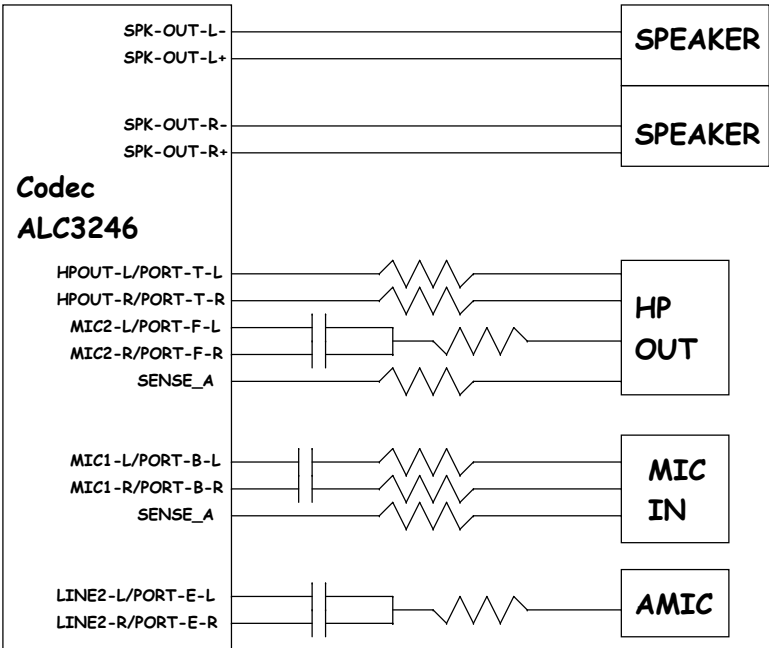


Thermal Block Diagram

TBD



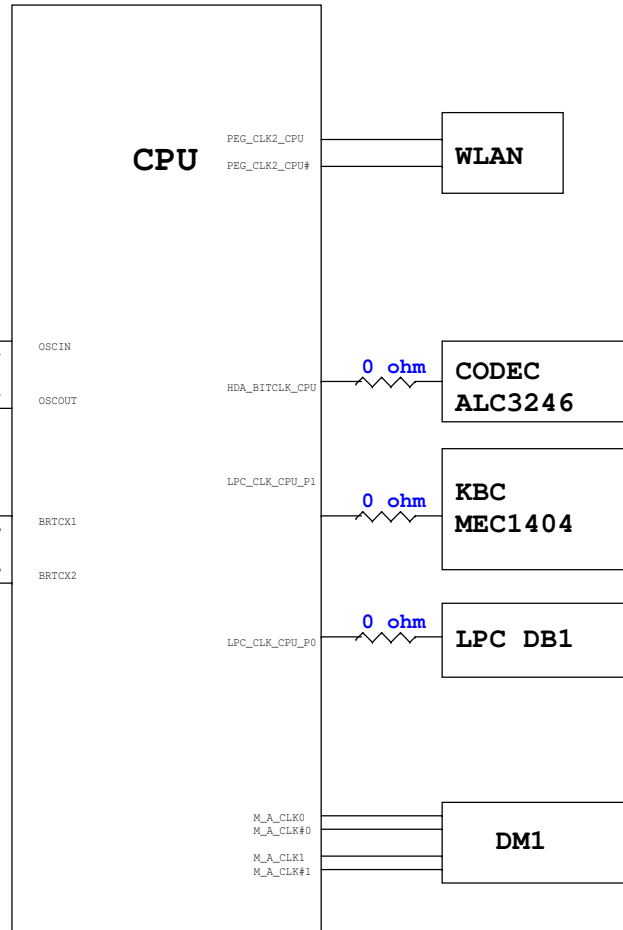
Audio Block Diagram TBD



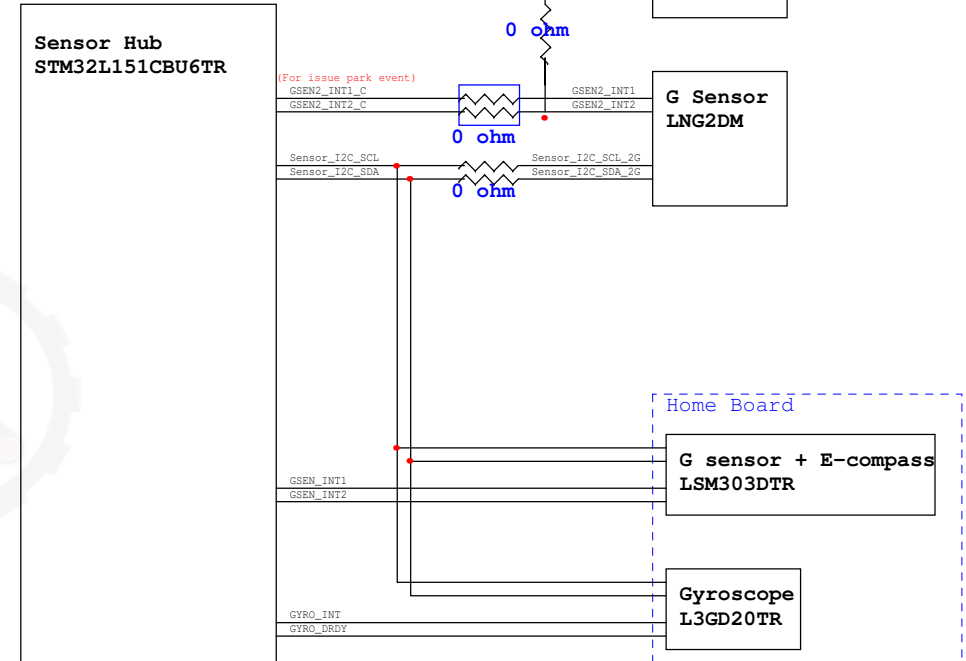
SSID = CLK Block Diagram

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TBD



TBD



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